1. INTRODUCTION

1.1. SUMMARY

The Rockwell RC2324DP/1 and RC2424DP/1 (referred to as the "DP/1") are each a single device, 2400 bps, full-duplex, modem data pump. The Rockwell RC2324DP/2 (referred to as the "DP/2") is a 2400 bps, full-duplex, modem data pump two-device set. The term "RC2324DP" refers to both capabilities of both the RC2324DP/1 and RC2324DP/2. In this document, the word "modem" refers to capabilities existing in all three modem data pumps unless otherwise stated.

The modem operates over the public switched telephone network (PSTN), as well as on point-to-point leased lines.

The modem meets the requirements specified in CCITT V.22 bis, V.22 A/B, and V.21, as well as Bell 212A and Bell 103. Also, CCITT V.23 is supported in the RC2324DP/1 and RC2324DP/2 but not in the RC2424DP/1.

SDLC/HDLC support eliminates the cost of an external serial input/output (SIO) device in products incorporating error correction protocols.

Each modem includes two CMOS VLSI functions—a digital signal processor (DSP) and an integrated analog function (IA). The DP/1 integrates these functions into a single device. The DP/2 supplies these functions in separate packages. The DP/1 modem includes the same hardware interface functions of the DP/2 modem except that eleven hardware signals are not provided on the DP/1: four serial control, two talk/data relay interface, two baud clock, and two internal test.

The DP/1 is available in a 68-pin plastic leaded chip carrier (PLCC).

The DP/2 is available as either a PLCC set or a quad in-line package (QUIP) and dual in-line package (DIP) set. The DSP is packaged in either a 68-pin PLCC or 64-pin QUIP. The IA is packaged in either a 44-pin PLCC or 40-pin DIP.

This document supports the following devices:

RC2324DP/1:
68-Pin PLCC		R6634-12 ("D" code)

RC2424DP/1:
68-Pin PLCC		R6634-13 ("D" code)

RC2324DP/2:
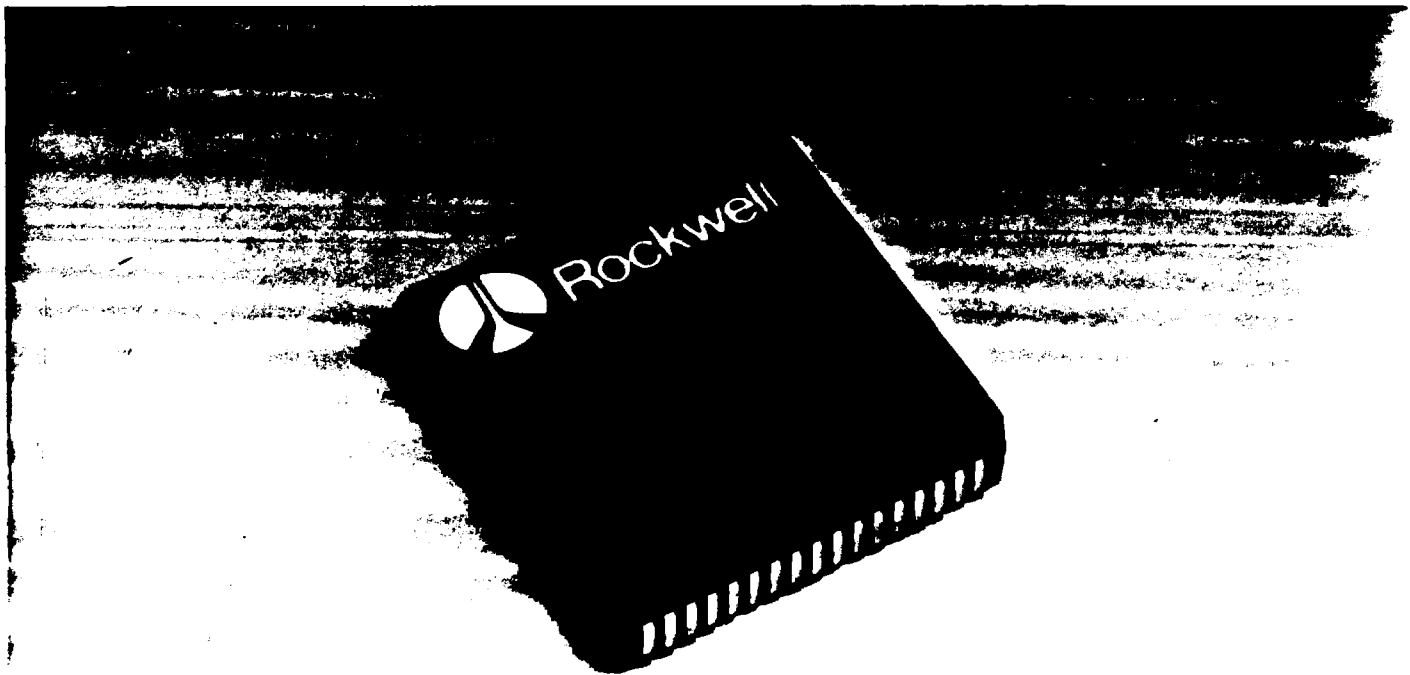|		
68-Pin PLCC	DSP	C5312-16 ("C" code)
68-Pin PLCC	DSP	C5312-20 ("D" code)
44-Pin PLCC	IA	10464-21
64-Pin QUIP	DSP	C5312-15 ("C" code)
64-Pin QUIP	DSP	C5312-19 ("D" code)
40-Pin DIP	IA	10464-20

Figure 1-1. RC2324DP/1 Modem In 68-Pin PLCC

1.2. FEATURES

- CMOS DSP and IA functions
- 2-wire full-duplex operation
- Compatible configurations:
    - CCITT V.22 bis, V.22A/B. V.21
    - Bell 212A and 103
    - CCITT V.23 (RC2324DP only)
- Receive dynamic range: –9 dBm to –43 dBm
- Maximum transmit level: 0.0 dBm ±1.0 dB, programmable in 1 dB steps
- Multi-modem detection support
    - Programmable tone detect bandpass filters
    - Zero-crossing detector
- V.22 bis fallback/fall-forward – 2400/1200 bps
- Serial data both synchronous and asynchronous
    - Synchronous:
      2400, 1200, 600 bps ±0.01% (PSK modulation)
      Internal/external/slave clock selection
    - Asynchronous:
      7, 8, 9, 10, or 11 bits per character
      2400, 1200, 600 bps +1%, –2.5%
      2.3% extended overspeed ("D" code only)
      (PSK modulation)
      0-300 bps (V.21 and Bell 103)
      75, 1200 bps (V.23 - RC2324DP only))
- Parallel data both synchronous and asynchronous
    - Synchronous:
      Normal sync: 8-bit data for transmit and receive
    - SDLC/HDLC support:
      Transmitter: Flag generation, 0 bit stuffing,
      CCITT CRC generation
      Receiver: Flag detection, 0 bit un-stuffing,
      CCITT CRC checking
    - Asynchronous:
      5, 6, 7, or 8 data bits per character
      Odd/even parity generation/checking
      (or 9th data bit)
      2400, 1200, 600 bps +1% (or 2.3%), –2.5%
      (PSK modulation)
      75, 300, 1200 bps (FSK modulation)
- Programmable ring detect
    - Min and max frequency range
- Programmable dialer
    - Make/break times for pulse dialling
    - DTMF on time for touch-tone dialling
    - Interdigit times for both pulse and tone dialling
    - DTMF Level: high tone level is 2.0 dB ± 0.5 dB above low tone level
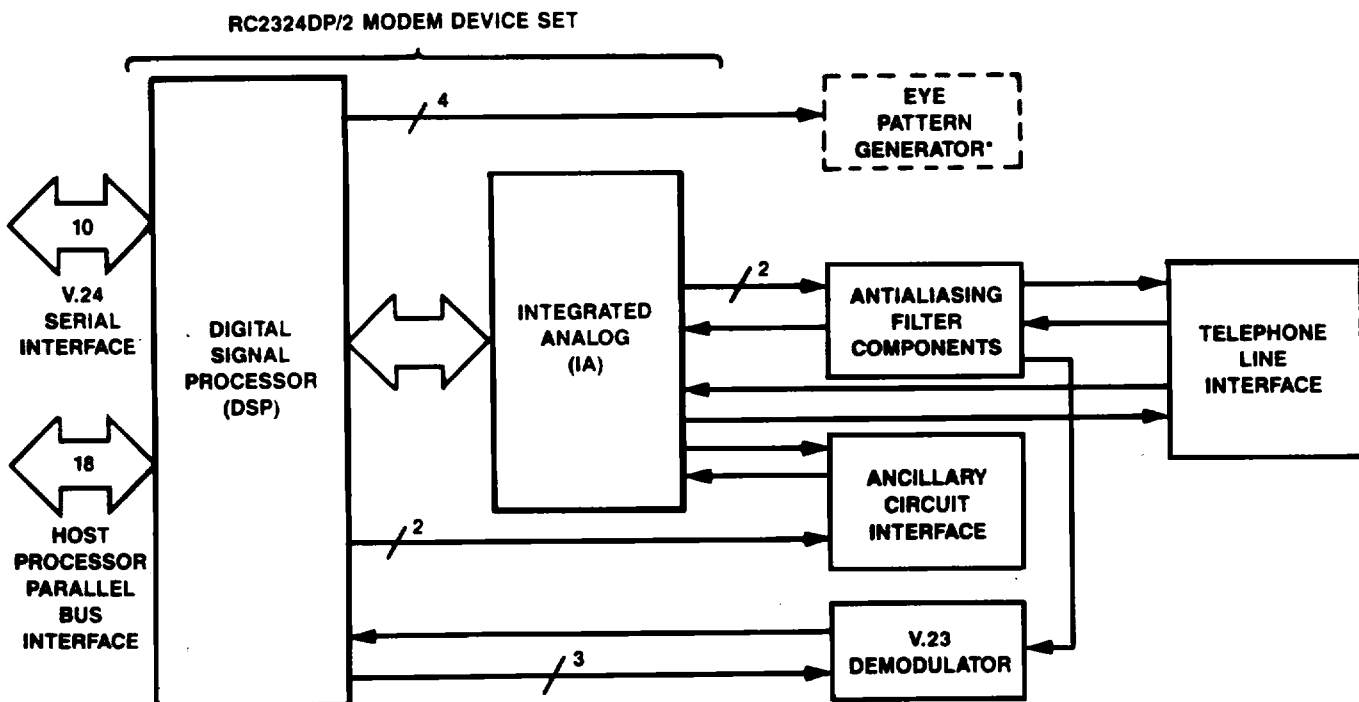
- Diagnostics
    - Read/write RAM
    - Serial eye pattern output
    - EQM value in RAM
- Host bus interface memory for configuration, control, and parallel data; compatible with an 8086 microprocessor bus
- Serial data interface (TTL compatible)
- Adaptive and fixed compromise equalization
- Test Configurations:
    - Local analog loopback
    - Local digital loopback
    - Remote digital loopback
- Answer and originate handshake
- Leased line operation
- Power requirements:
    - ± 5 Vdc ± 5%
    - 525 mW typical

1.3. GENERAL INTERFACE

The modem, with the addition of a few external filter components, interfaces easily to a data access arrangement (DAA). The modem general interface is illustrated in Figure 1-2.

a. RC2324DP/1 and RC2424DP/1

RC2324DP/2 MODEM DEVICE SET
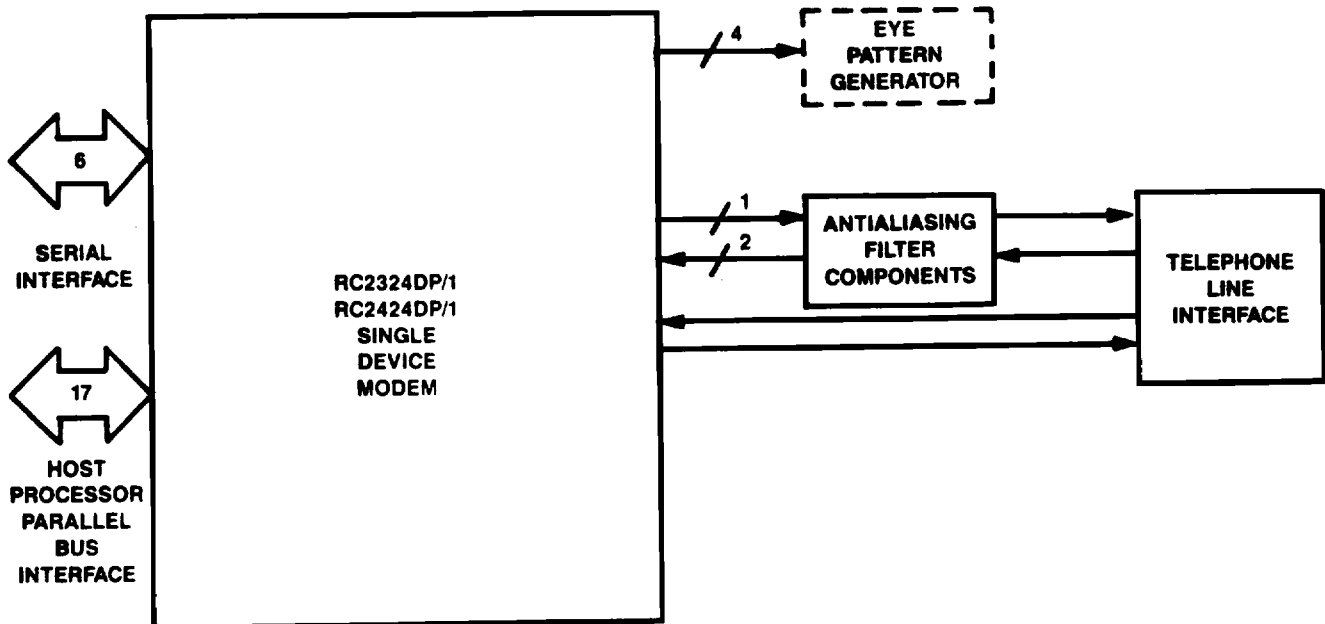
*FOR OPTIONAL DIAGNOSTIC USE

b. RC2324DP/2

Figure 1-2. Modem General Interface

1.4. TECHNICAL SPECIFICATIONS

CONFIGURATIONS, SIGNALING RATES, AND DATA RATES

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1-1. The modem configuration is established by the CONF bits.

Note: Bit names refer to control bits in DSP Interface Memory which are set or reset by the host processor (see Figure 3-1 and Table 3-1).

TONE GENERATION

Answer Tone: A CCITT (2100 ± 15 Hz) or Bell (2225 ± 10 Hz) answer tone is generated depending on the selected configuration.

Guard Tone: A guard tone of 1800 ± 20 Hz (GTS bit = 0) or 550 ± 20 Hz (GTS bit = 1) can be generated (enabled by the GTE bit). The level of transmitted power is 6 ± 1 dB or 3 ± 1 dB below the level of the data power in the main channel for the 1800 Hz or 550 Hz guard tone, respectively. The total power transmitted to the line is the same whether or not a guard tone is enabled. When a guard tone is generated, the main channel transmit path gain is reduced by 0.97 dB or 1.76 dB for the 1800 Hz or 550 Hz guard tone, respectively.

Guard tone on/off must be controlled by the host depending on the state of the handshake sequence, i.e., the host should enable guard tone when DSR is turned on.

DTMF Tones: When Dial/Call Progress configuration is selected (CONF bits = 81) and the DTMF bit is set to a 1, dual tone multi-frequency (DTMF) tones can be generated. The specific DTMF tone generated is specified by the host loading the Transmitter Data Buffer (TBUFFER) with the appropriate digit code shown in Table 1-2. (See Tone 1 Amplitude and Tone 2 Amplitude in Section 3.3.)

User Defined Tones: When Tone Generator/Tone Detector configuration is selected (CONF bits = 80), a user-defined single or dual tone can be generated. In this mode, the transmitter immediately begins sending the frequencies specified in DSP RAM. The tones will remain on as long as Tone Generator/Tone Detector configuration is selected and the tone amplitudes are greater than zero. Setting one of the two amplitudes to zero selects single tone frequency.

Note: Frequencies from 0 to 1675 Hz can be sent when the ORG bit is set, or frequencies from 1925 Hz to 2875 Hz can be sent when the ORG bit is cleared. 1800 Hz frequency can be sent by setting the GTE bit with GTS = 0 and ORG = 0.

Table 1-1. Configurations, Signaling and Data Rates

Configuration	Modulation[1]	Transmitter Carrier Frequency (Hz) ±0.01%		Data Rate (bps)	Baud	Bits Per	Constellation
		Answer[2]	Originate[2]	± 0.01%	(Symbols/Sec.)	Symbol	Points
V.22 bis	QAM	2400	1200	2400[3]	600	4	16
V.22A/B	DPSK	2400	1200	1200[3]	600	2	4
		2400	1200	600[3]	600	1	2
Bell 212A	DPSK	2400	1200	1200[3]	600	2	4
Bell 103	FSK	2225 M	1270 M	300[4]	300[4]	1	1
		2025 S	1070 S				
V.21	FSK	1650 M	980 M	300[4]	300[4]	1	1
		1850 S	1180 S				
V.23 Forward Channel[5]	FSK	1300 M	1300 M	1200	1200	1	1
		2100 S	2100 S				
V.23 Backward Channel[5]	FSK	390 M	390 M	75	75	1	1
		450 S	450 S				

Notes:
1. Modulation legend: QAM Quadrature Amplitude Modulation
   DPSK Differential Phase Shift Keying
   FSK Frequency Shift Keying
2. M indicates a mark condition; S indicates a space condition.
3. Synchronous accuracy = ±0.01%; asynchronous accuracy = −2.5% to +1.0% (+2.3% if extended overspeed is selected).
4. Value is upper limit for serial (e.g., 0-300).
5. RC2324DP only.

851C1

TONE DETECTION

Answer Tone and Call Progress Tones: When Dial/Call Progress configuration is selected (CONF bits = 81), tones can be detected as follows:

Call progress frequency range: 340 ± 5 Hz to 640 ± 5 Hz (status bit: TONEA)

Answer tones (2100 ± 15 Hz or 2225 ± 10 Hz) or Bell FSK originate tone (1270 ± 10 Hz) [status bits: ATV25, ATBELL (ORG=1), BEL103 (ORG=0)]

Detection range: 0 dBm to –43 dBm

Default detection threshold: –43 dBm

Response time: 25 ± 2 ms

Tones are detected as energy above a certain threshold within a digital bandpass filter. The pass band of the dual bi-quad infinite impulse response (IIR) filter (Call Progress) or the single bi-quad IIR filter (answer tone or Bell FSK originate) can be changed by writing new coefficients to DSP RAM. The tone detect threshold can also be changed in DSP RAM.

V.23 (RC2324DP only) and V.21 Tones: When Tone Generator/Tone Detector configuration is selected (CONF bits = 80), tones can be detected as follows:

V.23 forward channel mark: 1300 ± 10 Hz (status bit: TONEA) (RC2324DP only)

V.23 backward channel mark: 390 ± 10 Hz (status bit: TONEB) (RC2324DP only)

V.21 high band mark (1650 ± 10 Hz) or low band mark (980 ± 10 Hz) (status bit: TONEC)

Detection range: 0 dBm to –43 dBm

Default detection threshold: –43 dBm

Response time: 25 ± 2 ms

Tones are detected as energy above the threshold within a digital bandpass filter. These filters are single bi-quad IIR filters. The pass bands can be changed by writing new coefficients to DSP RAM. The tone detect threshold can also be changed in the DSP RAM.

Zero Crossing Detector: A zero crossing detector is always available. The detector can measure tone frequencies between 100 Hz and 3000 Hz. The zero crossing counter increments for both positive and negative zero crossings.

DATA ENCODING

The data encoding conforms to CCITT Recommendations V.22 bis, V.22A/B, V.23, or V.21, or to Bell 212A or 103, depending on the selected configuration.

EQUALIZERS

Equalization functions are incorporated that improve performance when operating over low quality lines.

Automatic Adaptive Equalizer. A 17-tap automatic adaptive equalizer is provided in the receiver circuit for V.22 bis, V.22 and Bell 212A configurations. Updating of the taps can be enabled or disabled (EQFZ bit). The equalizer taps can also be reset (EQRES bit).

Fixed Compromise Equalizer. A fixed compromise equalizer is provided in the transmitter. The equalizer can be enabled or disabled (CEQ bit).

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by a square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ± 150 microseconds over the frequency range 900 Hz to 1500 Hz (low channel) and 2100 Hz to 2700 Hz (high channel).

TRANSMIT LEVEL

The default transmitter output level is –6.0 dBm ±1.0 dB. The output level can be selected from 0 dBm to –15 dBm in 1 dB steps (TLVL bits).

TRANSMIT TIMING

Transmitter timing is selectable between internal (±0.01%), external, or loopback (TXCLK bits). When external clock is selected, the external clock rate must equal the desired data rate ±0.01% with a duty cycle of 50 ±20%.

Table 1-2. Dial Digits/Tone Pairs

Hex Code	Dial Digit	Tone Pair (Hz)	(Hz)
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	Spare (B)	697	1633
0C	Spare (C)	770	1633
0D	Spare (D)	852	1633
0E	#	941	1477
0F	Spare (F)	941	1633
10	1300 Hz Calling Tone		

SCRAMBLER/DESCRAMBLER

A self-synchronizing scrambler/descrambler satisfying the applicable CCITT recommendation or Bell specification is incorporated. The scrambler and descrambler can be enabled or disabled (SDIS and DDIS bits, respectively).

RECEIVE LEVEL

The receiver satisfies performance requirements for received line signals from –9 dBm to –43 dBm. The received line signal is measured at the Receiver Analog (RXA) input.

RECEIVER TIMING

The modem can track a ± 0.03% frequency error in the associated transmit timing source.

CARRIER RECOVERY

The modem can track a ±7 Hz frequency offset in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

SERIAL DATA INTERFACE

The serial data interface is supported by four bits in the DSP interface memory: CTS, DSR, RTS, and RLSD). In the DP/2, four hardware signals are also supported: CTS, DSR, RTS and RLSD.

RXD Clamping

Received Data (RXD) is clamped to a constant mark when the RLSD status bit is off (0).

RTS - CTS Response Time

The response times of CTS relative to a corresponding transition of RTS are listed in Table 1-3 for both constant carrier and controlled carrier mode (CC bit).

The CTS output follows the CTS bit by up to 4 baud in PSK synchronous modes.

For V.23 half-duplex mode (1200 bps), it is recommended that the RTS ON to CTS ON timing be extended by the host from 11 ms to 20-40 ms (RC2324DP only).

Table 1-3. RTS-CTS Response Time

CTS Transition	Configuration	Constant Carrier	Controlled Carrier
OFF to ON	V.22 bis	≤2 ms	270 ms
	V.22	≤2 ms	270 ms
	Bell 212A	≤2 ms	270 ms
	V.21	2-5 ms	2-5 ms
	Bell 103	2-5 ms	2-5 ms
	V.23	11 ms	11 ms
ON to OFF	All	≤2 ms	≤2 ms

ASYNC/SYNC, SYNC/ASYNC CONVERSION

An asynchronous-to-synchronous converter is provided in the transmitter, and a synchronous-to-asynchronous converter is provided in the receiver. Asynchronous or synchronous mode is selected by the ASYNC bit. The asynchronous character format is 1 start bit, 5 to 8 data bits (WDSZ bits), an optional parity bit (PARSL and PEN bits), and 1 or 2 stop bits (STB bit). Valid character sizes, including all bits, are 7, 8, 9, 10 or 11 bits per character.

When the transmitter's converter is operating at the basic signalling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters.

Parallel Mode Signalling Rate Range. Two ranges of signalling rates are provided in parallel mode (selectable by the EXOS bit):

Basic range: +1% to –2.5%

Extended overspeed range: +2.3% to –2.5%

Extended overspeed in V.22 and V.22 bis parallel data modes is fully supported up to 2.3% (CCITT limit). However, if the host relies totally on the Transmitter Data Buffer Empty bit (TDBE) interrupt timing for the host data input timing, then the actual data rate may exceed the 2.3% limit, which is not permitted. Therefore, in this mode the host must keep the speed within the 2.3% tolerance.

Note: The above discussion does not apply to the normal overspeed (1.0%) case. For this mode, TDBE interrupt timing can be relied on to input data to the modem, in which case the modem will transmit at the overspeed rate. The host can enable extended overspeed in the receiver while transmitting data at the basic overspeed rate by setting the SPLIT bit.

Serial Mode Signalling Rate Range. Two ranges of signalling rates are provided in serial mode (selectable by the EXOS bit):

Basic range: +1% to –2.5%

Extended overspeed range: +2.3% to –2.5%
("D" code only)

Break. Break is handled in the transmitter and receiver as described in V.22 bis. If the modem transmitter detects M to 2M + 3 bits of "start" polarity from the DTE, where M is the number of bits per character, the modem will transmit 2M + 3 bits of start polarity. If the modem detects more then 2M +3 bits of start polarity, it will transmit all these bits as start polarity.

The modem receiver will output the 2M + 3 or more bits of start polarity on RXD and will set the BRKD bit.

POWER REQUIREMENTS

The power requirements are specified in Table 1-4.

ENVIRONMENTAL SPECIFICATIONS

The environmental specifications are listed in Table 1-5.

Table 1-4. Modem Power Requirements

Voltage	Tolerance	Current (Typ.) @ 25°C	Current (Max.) @ 0°C
+ 5 VDC	±5%	85 mA	130 mA
– 5 VDC	±5%	20 mA	40 mA

Note: Input voltage ripple ≤ 0.1 volts peak-to-peak. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 microvolts peak.

Table 1-4. Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to + 70°C (32°F to 158° F)
Storage	– 40°C to + 80°C (–40°F to 176°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	– 200 feet to +10,000 feet

1.5. COMPATIBILITIES

1.5.1. RC2324DP/2 TO R2424DS COMPATIBILITY

A high performance modem engine, the RC2324DP/2 is the functional and performance equivalent of Rockwell's R2424DS modem with the following enhancements:

—2-device implementation in CMOS

—V.21 interface

— V.23 (RC2324DP only) interface

—Asynchronous/synchronous parallel data transfer over the microprocessor bus interface

—Extended 2.3% overspeed in asynchronous, DPSK/QAM modes

—SDLC/HDLC framing in parallel data mode

—Additional configuration and control capabilities

These options and enhancements, combined with a user accessible, dual port interface memory (RAM) in the DSP, offer maximum flexibility in customizing the modem to meet a wide variety of functional requirements.

1.5.2. RC2324DP/1 TO RC2324DP/2 COMPATIBILITY

The RC2324DP/1 is the functional and performance equivalent of the RC2324DP/2 with the following differences:

—Single device rather than two-device set

—The host must initialize the PKGSEL bit in the DSP interface memory to a 1 during reset processing (see Table 3-1).

—Serial data transfer hardware control signals ($\overline{CTS}$, $\overline{DSR}$, $\overline{RTS}$, and $\overline{RLSD}$) are not available (equivalent bits in DSP interface memory are available).

—Talk/Data relay driver output and control input hardware signals are not available.

—RBCLK and TBCLK output hardware signals are not available.

2. HARDWARE INTERFACE

2.1. PIN ASSIGNMENTS

RC2324DP/1 and RC2424DP/1. The DP/1 pin assignments are shown in Figure 2-1. The pin assignments are listed by pin number in Table 2-1.

RC2324DP/2. The RC2324DP/2 pin assignments are shown in Figure 2-2. The pin assignments are listed by pin number in Tables 2-2 and 2-3 for the DSP and IA devices, respectively.
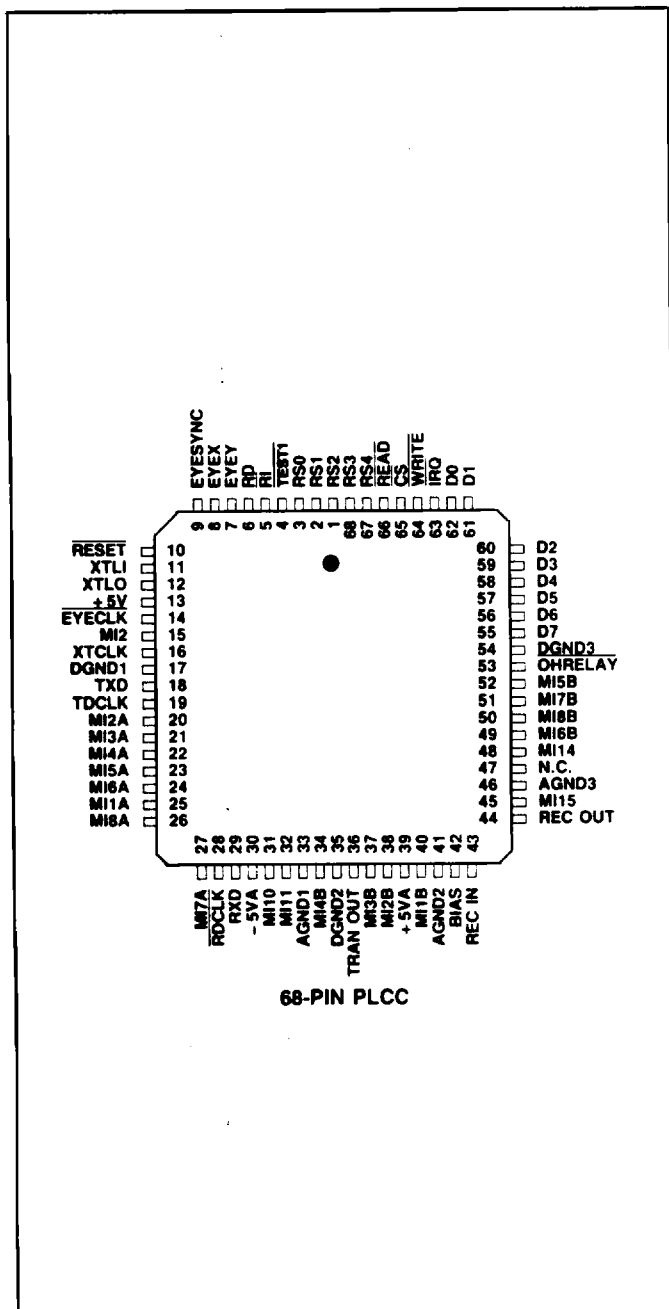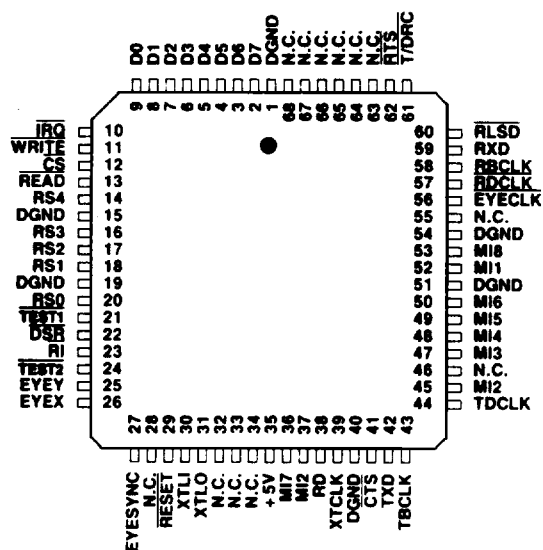

Figure 2-1. RC2324DP/1 and RC2424DP/1 Pin Signals

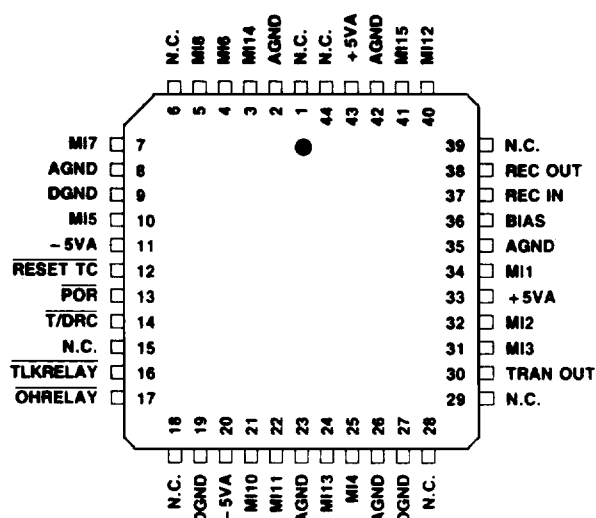**Table 2-1. RC2324DP/1 and RC2424DP/1 Pin Signals**

Pin Number	Signal Name	I/O Type
1	RS2	IA
2	RS1	IA
3	RS0	IA
4	TEST1	
5	RI	OB
6	RD	IA
7	EYEY	OB
8	EYEX	OB
9	EYESYNC	OB
10	RESET	IA
11	XTLI	I
12	XTLO	O
13	+5V	
14	EYECLK	OA
15	MI2	
16	XTCLK	IA
17	DGND1	
18	TXD	IA
19	TDCLK	OA
20	MI2A	TO MI2B(38)
21	MI3A	TO MI3B(37)
22	MI4A	TO MI4B(34)
23	MI5A	TO MI5B(52)
24	MI6A	TO MI6B(49)
25	MI1A	TO MI1B(40)
26	MI8A	TO MI8B(50)
27	MI7A	TO MI7B(51)
28	RDCLK	OA
29	RXD	OA
30	–5VA	
31	MI10	
32	MI11	
33	AGND1	
34	MI4B	TO MI4A(22)
35	DGND2	
36	TRAN OUT	O (DD)
37	MI3B	TO MI3A (21)
38	MI2B	TO MI2A (20)
39	+5VA	
40	MI1B	TO MI1A (25)
41	AGND2	
42	BIAS	I
43	REC IN	I (DB)
44	REC OUT	O (DA)
45	MI15	
46	AGND3	
47	NC	
48	MI14	
49	MI6B	TO MI6A (24)
50	MI8B	TO MI8A (26)
51	MI7B	TO MI7A (27)
52	MI5B	TO MI5A (23)
53	OHRELAY	OD
54	DGND3	
55	D7	IA/OB
56	D6	IA/OB
57	D5	IA/OB
58	D4	IA/OB
59	D3	IA/OB
60	D2	IA/OB
61	D1	IA/OB
62	D0	IA/OB
63	IRQ	OC
64	WRITE	IA
65	CS	IA
66	READ	IA
67	RS4	IA
68	RS3	IA

Notes: 1. MI = Modem Interconnection (e.g., MI7), see Figure 8-1.
2. N.C. = No Connection, leave pin disconnected (open).
3. I/O Type: See Tables 2-5 and 2-6.
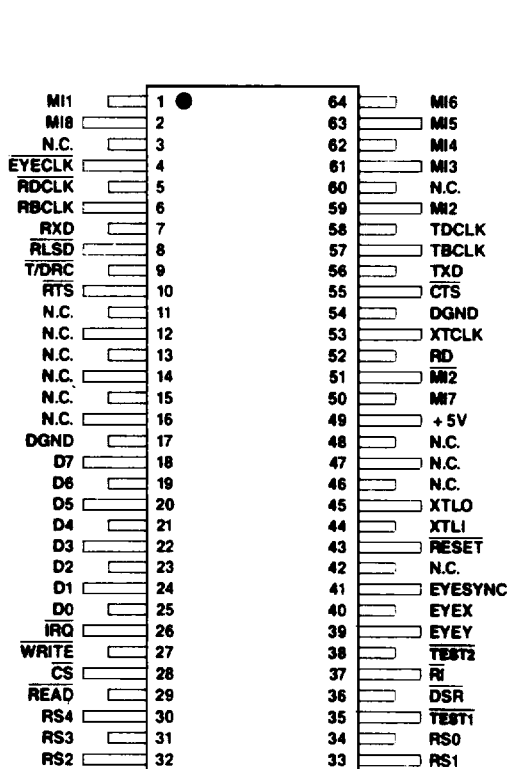4. Connect TEST1 input to +5V through a 10 KΩ resistor.
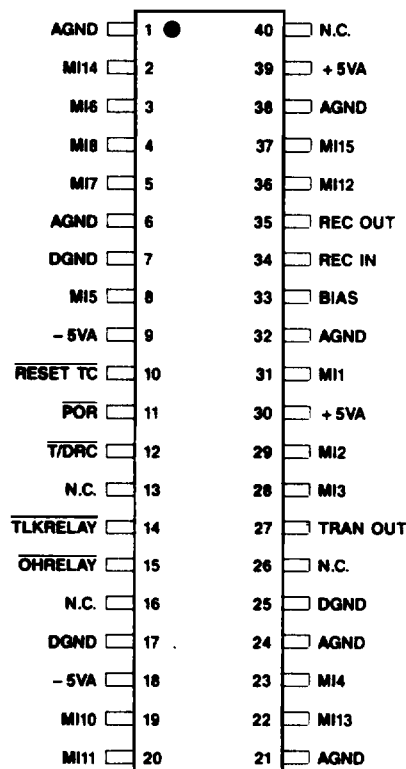
68-PIN PLCC

IRQ	10	
WRITE	11	
CS	12	
READ	13	
RS4	14	
DGND	15	
RS3	16	
RS2	17	
RS1	18	
DGND	19	
RS0	20	
TEST1	21	
DSR	22	
RI	23	
TEST2	24	
EYEY	25	
EYEX	26	

Top pins: D0, D1, D2, D3, D4, D5, D6, D7, DGND, N.C., N.C., N.C., N.C., N.C., RTS, T/DRC

Right pins: 60 RLSD, 59 RXD, 58 RBCLK, 57 RDCLK, 56 EYECLK, 55 N.C., 54 DGND, 53 MI8, 52 MI1, 51 DGND, 50 MI6, 49 MI5, 48 MI4, 47 MI3, 46 N.C., 45 MI2, 44 TDCLK

Bottom pins (27–43): EYESYNC, N.C., RESET, XTLI, XTLO, N.C., N.C., +5V, MI7, MI2, RD, XTCLK, DGND, CTS, TXD, TBCLK

44-PIN PLCC

MI7	7	
AGND	8	
DGND	9	
MI5	10	
-5VA	11	
RESET TC	12	
POR	13	
T/DRC	14	
N.C.	15	
TLKRELAY	16	
OHRELAY	17	

Top pins: N.C., MI8, MI6, MI14, AGND, N.C., N.C., +5VA, AGND, MI15, MI12

Right pins: 39 N.C., 38 REC OUT, 37 REC IN, 36 BIAS, 35 AGND, 34 MI1, 33 +5VA, 32 MI2, 31 MI3, 30 TRAN OUT, 29 N.C.

Bottom pins (18–28): N.C., DGND, -5VA, MI10, MI11, AGND, MI13, MI4, AGND, DGND, N.C.

a. PLCC

64-PIN QUIP (DSP)

Left	Pin	Pin	Right
MI1	1	64	MI6
MI8	2	63	MI5
N.C.	3	62	MI4
EYECLK	4	61	MI3
RDCLK	5	60	N.C.
RBCLK	6	59	MI2
RXD	7	58	TDCLK
RLSD	8	57	TBCLK
T/DRC	9	56	TXD
RTS	10	55	CTS
N.C.	11	54	DGND
N.C.	12	53	XTCLK
N.C.	13	52	RD
N.C.	14	51	MI2
N.C.	15	50	MI7
N.C.	16	49	+5V
DGND	17	48	N.C.
D7	18	47	N.C.
D6	19	46	N.C.
D5	20	45	XTLO
D4	21	44	XTLI
D3	22	43	RESET
D2	23	42	N.C.
D1	24	41	EYESYNC
D0	25	40	EYEX
IRQ	26	39	EYEY
WRITE	27	38	TEST2
CS	28	37	RI
READ	29	36	DSR
RS4	30	35	TEST1
RS3	31	34	RS0
RS2	32	33	RS1

40-PIN DIP (IA)

Left	Pin	Pin	Right
AGND	1	40	N.C.
MI14	2	39	+5VA
MI6	3	38	AGND
MI8	4	37	MI15
MI7	5	36	MI12
AGND	6	35	REC OUT
DGND	7	34	REC IN
MI5	8	33	BIAS
-5VA	9	32	AGND
RESET TC	10	31	MI1
POR	11	30	+5VA
T/DRC	12	29	MI2
N.C.	13	28	MI3
TLKRELAY	14	27	TRAN OUT
OHRELAY	15	26	N.C.
N.C.	16	25	DGND
DGND	17	24	AGND
-5VA	18	23	MI4
MI10	19	22	MI13
MI11	20	21	AGND

a. QUIP/DIP

Figure 2-2. RC2324DP/2 Pin Signals

Table 2-2. RC2324DP/2 DSP Pin Signals

68-Pin PLCC Pin Number	64-Pin QUIP Pin Number	Signal Name	I/O Type
52	1	MI1	
53	2	MI8	
54	–	DGND	
55	3	N.C.	
56	4	EYECLK	OA
57	5	RDCLK	OA
58	6	RBCLK	OA
59	7	RXD	OA
60	8	RLSD	OA
61	9	T/DRC	IA
62	10	RTS	IA
63	11	N.C.	
64	12	N.C.	
65	13	N.C.	
66	14	N.C.	
67	15	N.C.	
68	16	N.C.	
1	17	DGND	
2	18	D7	IA/OB
3	19	D6	IA/OB
4	20	D5	IA/OB
5	21	D4	IA/OB
6	22	D3	IA/OB
7	23	D2	IA/OB
8	24	D1	IA/OB
9	25	D0	IA/OB
10	26	IRQ	OC
11	27	WRITE	IA
12	28	CS	IA
13	29	READ	IA
14	30	RS4	IA
15	–	DGND	
16	31	RS3	IA
17	32	RS2	IA
18	33	RS1	IA
19	–	DGND	
20	34	RS0	IA
21	35	TEST1	I
22	36	DSR	OB
23	37	RI	OB
24	38	TEST2	I
25	39	EYEY	OB
26	40	EYEX	OB
27	41	EYESYNC	OB
28	42	N.C.	
29	43	RESET	ID
30	44	XTLI	I
31	45	XTLO	O
32	46	N.C.	
33	47	N.C.	
34	48	N.C.	
35	49	+5V	
36	50	MI7	
37	51	MI2	
38	52	RD	IA
39	53	XTCLK	IA
40	54	DGND	
41	55	CTS	OA
42	56	TXD	IA
43	57	TBCLK	OA
44	58	TDCLK	OA
45	59	MI2	
46	60	N.C.	
47	61	MI3	
48	62	MI4	
49	63	MI5	
50	64	MI6	
51	–	DGND	

Notes: 1. MI = Modem Interconnection (e.g., MI7), see Figure 8-1.
2. N.C. = No Connection, leave pin disconnected (open).
3. I/O Type: See Table 2-5.
4. Tie TEST1 and TEST2 inputs to +5V through a 10 KΩ resistor.

Table 2-3. RC2324DP/2 IA Pin Signals

44-Pin PLCC Pin Number	40-Pin DIP Pin Number	Signal Name	I/O Type
1	–	N.C.	
2	1	AGND	
3	2	MI14	
4	3	MI6	
5	4	MI8	
6	–	N.C.	
7	5	MI7	
8	6	AGND	
9	7	DGND	
10	8	MI5	
11	9	–5VA	
12	10	RESET TC	IA
13	11	POR	IA/OA
14	12	T/DRC	IA
15	13	N.C.	
16	14	TLKRELAY	OD
17	15	OHRELAY	OD
18	16	N.C.	
19	17	DGND	
20	18	–5VA	
21	19	MI10	
22	20	MI11	
23	21	AGND	
24	22	MI13	
25	23	MI4	
26	24	AGND	
27	25	DGND	
28	–	N.C.	
29	26	N.C.	
30	27	TRAN OUT	O (DD)
31	28	MI3	
32	29	MI2	
33	30	+5VA	
34	31	MI1	
35	32	AGND	
36	33	BIAS	I
37	34	REC IN	I (DB)
38	35	REC OUT	O (DA)
39	–	N.C.	
40	36	MI12	
41	37	MI15	
42	38	AGND	
43	39	+5VA	
44	40	N.C.	

Notes: 1. MI = Modem Interconnection (e.g., MI7), see Figure 8-1.
2. N.C. = No Connection, leave pin disconnected (open).
3. I/O Type: See Tables 2-5 and 2-6.

2.2. HARDWARE INTERFACE SIGNALS

The functional hardware interface signals for the DP/1 and the DP/2 are shown in Figures 2-3 and 2-4, respectively. In these diagrams, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., IRQ). Active low signals are overscored (e.g., POR).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., RDCLK), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The hardware interconnect signals are organized into functional groups. These signals, along with their interface circuit type codes, are listed in Table 2-4. The digital and analog interface characteristics are defined in Tables 2-5 and 2-6, respectively.

The hardware interface signals are defined in Table 2-7.
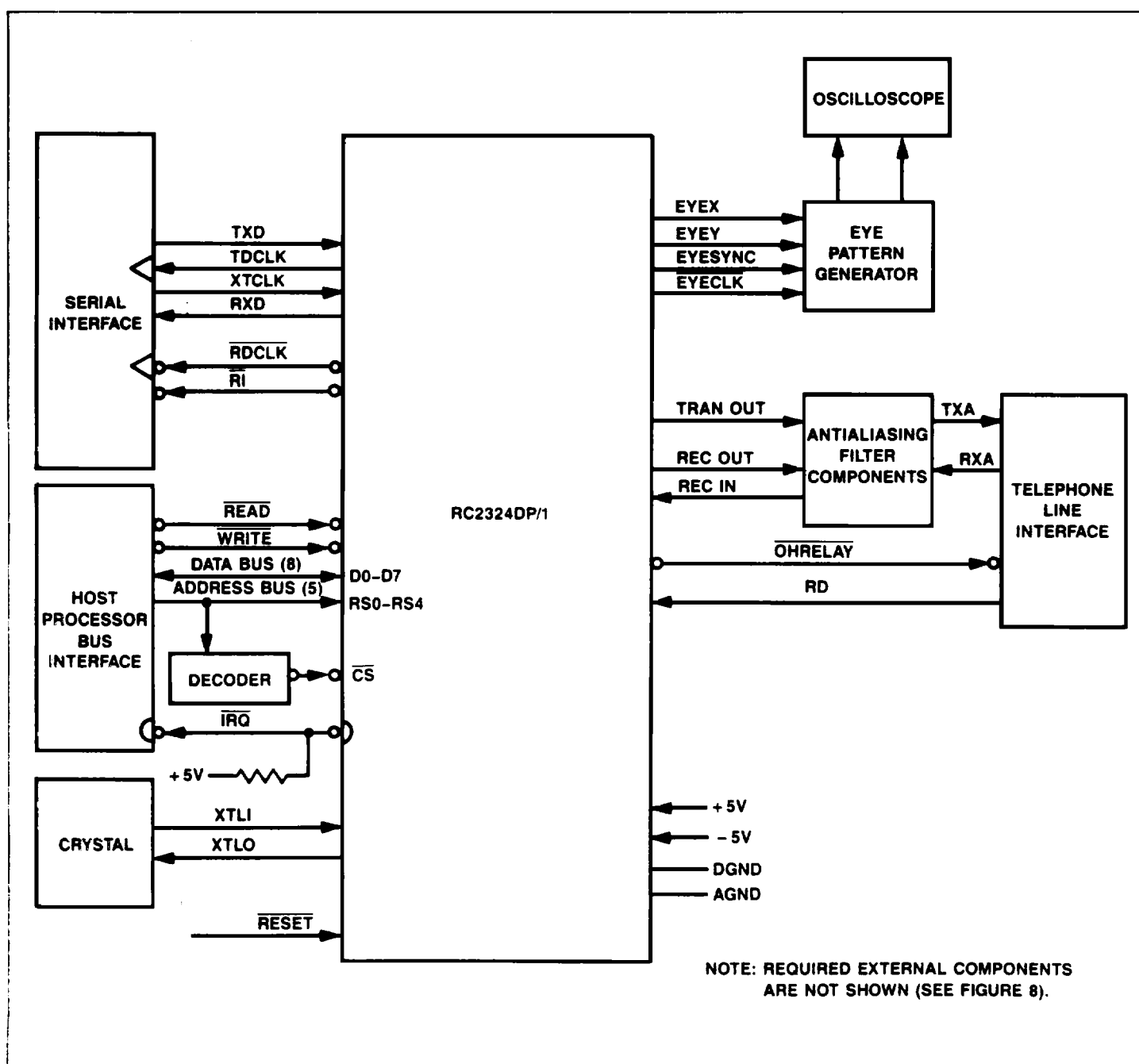
Figure 2-3. RC2324DP/1 and RC2424DP/1 Interface Signals

851C2
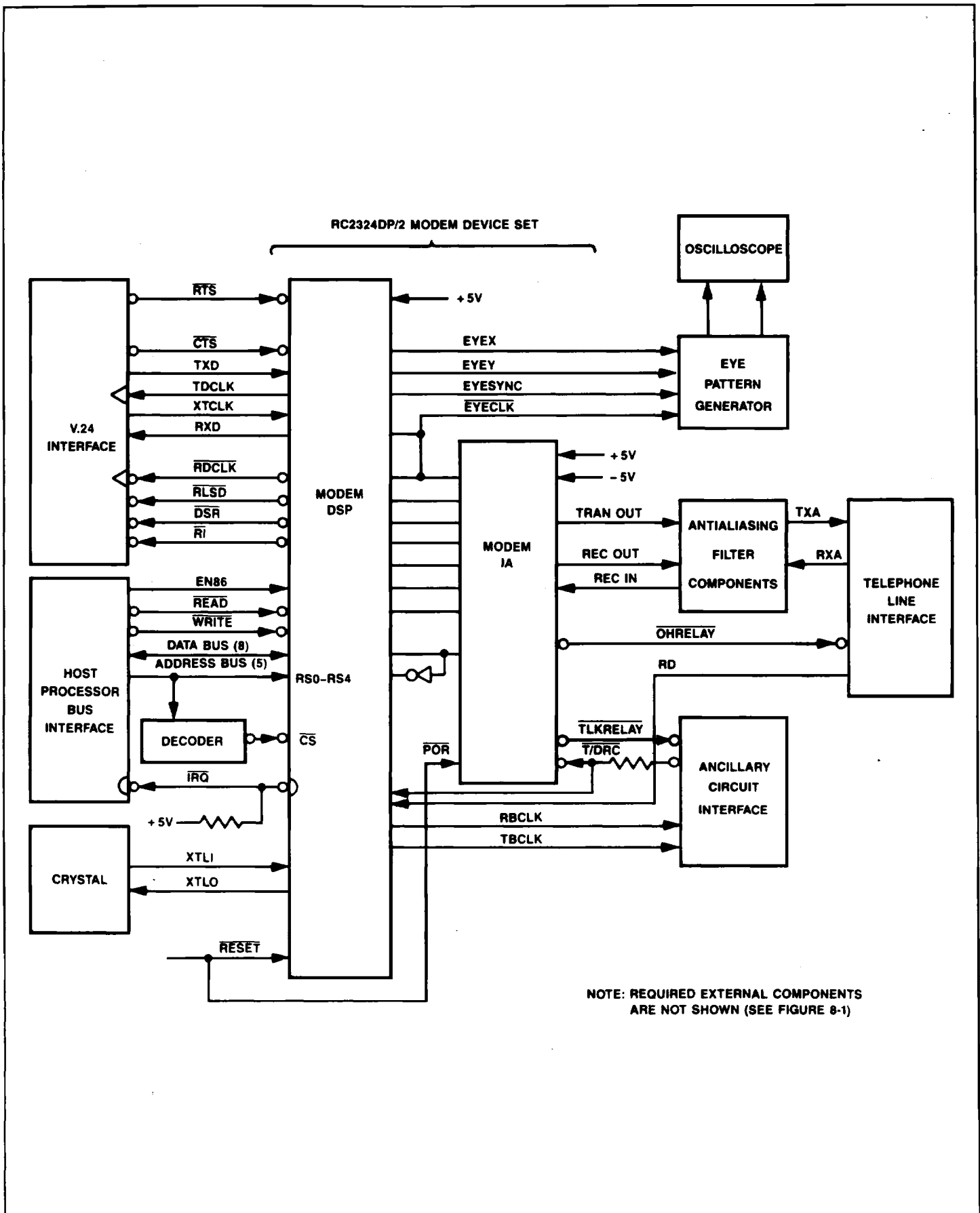
Figure 2-4. RC2324DP/2 Interface Signals

Table 2-4. Hardware Interface Signals

Name	I/O Type[1]	Description	Notes
Overhead			
XTLI	I	Crystal In	
XTLO	O	Crystal Out	
RESET	ID	Reset (DSP)	
POR	IA/OA	Power-On-Reset (IA)	2
RESET TC	IA	Reset Time Constant (IA)	2
+5V	PWR	+5 Volt Supply	
–5V	PWR	–5 Volt Supply	
AGND	GND	Analog Ground Return	
DGND	GND	Digital Ground Return	
TEST1	I	Factory Test	5
TEST2	I	Factory Test	2,5
DSP/Host Processor Parallel Bus Interface			
D7	IA/OB	Data Bus Line 7	
D6	IA/OB	Data Bus Line 6	
D5	IA/OB	Data Bus Line 5	
D4	IA/OB	Data Bus Line 4	
D3	IA/OB	Data Bus Line 3	
D2	IA/OB	Data Bus Line 2	
D1	IA/OB	Data Bus Line 1	
D0	IA/OB	Data Bus Line 0	
RS4	IA	Register Select Line 4	
RS3	IA	Register Select Line 3	
RS2	IA	Register Select Line 2	
RS1	IA	Register Select Line 1	
RS0	IA	Register Select Line 0	
CS	IA	Chip Select	
READ	IA	Read Enable	
WRITE	IA	Write Enable	
IRQ	OC	Interrupt Request	
DSP/Serial Interface			
TXD	IA	Serial Transmit Data	
RXD	OA	Serial Receive Data	
TDCLK	OA	Transmitter Data Clock	
XTCLK	IA	External Transmit Clock	
RDCLK	OA	Receiver Data Clock	
RI	OB	Ring Indicator	
RTS	IA	Request-To-Send	2
CTS	OA	Clear-To-Send	2
DSR	OA	Data Set Ready	2
RLSD	OA	Received Line Signal Detector	2

Table 2-4. Hardware Interface Signals (Cont'd)

Name	I/O Type[1]	Description	Notes
Modem/External Filter Components			
REC IN	DB	IA Receiver Op Amp Input	
REC OUT	DA	IA Receiver Op Amp Output	
TRAN OUT	DD	IA Transmitter Analog Output	
External Filter Components/Line Interface			
RXA	DE	Receive Analog Input	
TXA	DF	Transmit Analog Output	
Modem/Line Interface			
OHRELAY	OD	Off-Hook Relay Driver	
RD	IA	Ring Detect	
Modem/Ancillary Circuits			
TBCLK	OA	Transmit Baud Clock	2
RBCLK	OA	Receive Baud Clock	2
T/DRC	IA	Uncommitted Relay Control	2
TLKRELAY	OD	Uncommitted Relay Driver	2
DSP/Eye Pattern Generator (Diagnostic Circuit)			
EYEX	OB	Eye Pattern Data X-Axis	
EYEY	OB	Eye Pattern Data Y-Axis	
EYECLK	OA	Eye Pattern Clock	
EYESYNC	OB	Eye Pattern Sync	

Notes:

1. I/O types are described in Table 2-5 (digital signals) and Table 2-6 (analog signals).
2. RC2324DP/2 only.
3. RC2324DP/1 only.
4. Unused inputs tied to +5V or ground require individual 10K Ω series resistors.
5. Tie TEST1 and TEST2 inputs to +5V through 10K Ω resistor.

Table 2-5. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage Types IA and IB Type ID	V_{IH}	 2.0 0.8(V_{CC})	 – –	 V_{CC} V_{CC}	Vdc	
Input High Current	I_{IH}	–	–	40	μA	V_{CC} = 5.25V, V_{IN} = 5.25V
Input Low Voltage	V_{IL}	–0.3	–	0.8	Vdc	
Input Low Current	I_{IL}	–	–	–400	μA	V_{CC} = 5.25V
Input Leakage Current	I_{IN}	–	–	±2.5	μA	V_{IN} = 0 to +5V, V_{CC} = 5.25V
Output High Voltage Types OA and OB Type OD	V_{OH}	 3.5 –	 – –	 – V_{CC}	Vdc	 I_{LOAD} = – 100 μA I_{LOAD} = 0 mA
Output Low Voltage Types OA and OC Type OB Type OD	V_{OL}	 – – –	 – – 	 0.4 0.4 0.75	Vdc	 I_{LOAD} = 1.6 mA I_{LOAD} = 0.8 mA I_{LOAD} = 15 mA
Three–State Input Current (Off)	I_{TSI}	–	–	±10	μA	V_{IN} = 0.4 to V_{CC} –1
Power Dissipation	P_D	–	525	850	mW	

Table 2-6. Analog Interface Characteristics

Name	Type	Characteristic
REC OUT	DA	1458 type op amp output Dynamic range: –9 dBm to –43 dBm
REC IN	DB	1458 type op amp input
TRAN OUT	DD	1458 type op amp output: P_O (High Band) = –0.5 dBm P_O (Low Band) = –2.5 dBm
RXA	DE	Input impedance: 23.7 KΩ ± 1% Maximum receive level: –9 dBm
TXA	DF	1458 type op amp output Maximum output level (unloaded): 0 dBm ±1 dB

Table 2-7. Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI XTLO	I	**Crystal In and Crystal Out.** The DSP must be connected to an external crystal circuit consisting of a 24.00014 MHz crystal and two capacitors, a square wave generator, or a sine wave oscillator (see Figure 8-1).
$\overline{RESET}$	ID	**Reset.** The active low $\overline{RESET}$ input resets the internal modem logic. Upon transition of $\overline{RESET}$ from low-to-high, the DSP interface memory bits are set to the default values shown in Table 3-1. During modem power turn-on, $\overline{RESET}$ must be held low for at least 1ms after V_{CC} attains operating voltage. The modem is ready for use 350 ms after the low-to-high transition of $\overline{RESET}$.
$\overline{POR}$	IA/OA	**Power-On-Reset (DP/2 Only).** The IA Power-On Reset ($\overline{POR}$) signal is a bidirectional signal that is used as an active low input to reset the IA device and as an active low output to initiate an external reset of the DSP when a low power condition is detected within the IA device.
		The IA device power-on reset circuit monitors the IA +5V supply and outputs a 100 ms to 300 ms low pulse on $\overline{POR}$ upon IA +5V turn-on. This pulse is generated regardless of the IA –5V supply level. A 10 ms minimum low pulse on $\overline{POR}$ is also generated when the IA +5V supply drops below 3.5V.
		The DSP $\overline{RESET}$ input is usually tied to the IA $\overline{POR}$ line to have the IA $\overline{POR}$ output initiate a reset upon modem power turn-on or if the IA detects a low power condition.
		When DSP $\overline{RESET}$ and IA $\overline{POR}$ are tied together, the IA devices pulses $\overline{POR}$ low upon IA power turn-on to begin the $\overline{POR}$ sequence. The modem is ready 350 ms after the low-to-high transition of $\overline{POR}$. The $\overline{POR}$ sequence is reinitiated any time the +5V supply drops below +3.5V for more than 30 ms, or an external device drives $\overline{POR}$ low for at least 3 µs. POR is not pulsed low by the IA device when the $\overline{POR}$ sequence is initiated externally.
		NOTE: If the modem is used in applications where the supply voltage can drop below +4.75V but not low enough to cause a $\overline{POR}$ sequence (i.e., <+3.5V), the host system should assert the reset signals to the DSP and IA devices upon supply voltage recovery to ensure proper modem initialization and operation.
$\overline{RESET\ TC}$	IA	**IA Reset Time Constant (DP/2 Only).** When IA $\overline{POR}$ is used as described above, an external discrete RC network must be connected to the $\overline{RESET\ TC}$ pin to generate the $\overline{POR}$ long time constant (see Figure 7-1b).
		In modem circuits not requiring the bidirectional $\overline{POR}$ signal, the $\overline{RESET\ TC}$ input can be used as the active low reset input to the IA device rather than $\overline{POR}$. In this case, the $\overline{RESET\ TC}$ should be connected to the DSP $\overline{RESET}$ input instead of the RC network, and the IA $\overline{POR}$ input should be left open.
+5V	PWR	**+ 5V Supply.** +5V ± 5% is required.
–5V	PWR	**–5V Supply.** –5V ± 5% is required.
DGND	GND	**Digital Ground.**
AGND	GND	**Analog Ground.**

Table 2-7. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		MICROPROCESSOR INTERFACE
		Address, data, control and interrupt hardware interface signals implement an 8086-compatible parallel microprocessor interface to a host processor. This parallel interface allows the host to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits.
		The read/write cycle timing requirements are listed in Table 2-8 and the timing waveforms are illustrated in Figure 2-5. The definitions of the control and status bits, along with the methods of data interchange, are discussed in Section 3.
D0–D7	IA/OA	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable (READ) and Write Enable (WRITE) signals.
$\overline{CS}$	IA	**Chip Select.** The active low Chip Select ($\overline{CS}$) input selects the modem DSP for parallel data transfer between the DSP and the host over the microprocessor bus.
RS0 - RS4	IA	**Register Select Lines.** The five active high Register Select inputs (RS0 - RS4) address interface memory registers within the DSP when $\overline{CS}$ is low. These lines are typically connected to address lines A0-A4.
		When selected by $\overline{CS}$ low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00-1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0-D7).
$\overline{READ}$, $\overline{WRITE}$	IA	**Read Enable and Write Enable.** Reading or writing is controlled by the host pulsing either $\overline{READ}$ or $\overline{WRITE}$ input low, respectively, during the microprocessor bus access cycle (Figure 2-5a).
		During a read cycle, data from the addressed DSP interface memory register is gated onto the data bus by means of tri-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the tri-state drivers assume their high-impedance (off) state.
		During a write cycle, data from the data bus is copied into the addressed DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
$\overline{IRQ}$	OA	**Interrupt Request.** The modem Interrupt Request ($\overline{IRQ}$) output may be connected to the host interrupt request input in order to interrupt host program execution for immediate modem service. The IRQ output can be enabled in the DSP interface memory to indicate immediate change of conditions in the modem DSP device. The use of $\overline{IRQ}$ is optional depending upon modem application. Refer to the Software Considerations Section for a summary of the modem interrupt bits, interrupt conditions and interrupt clearing procedures.
		The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). The $\overline{IRQ}$ output can be wire-ORed with other IRQ lines in the application system. Any of these sources can drive the host interrupt request input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high).
		Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the IRQ line high when all IRQ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25W, is sufficient.

Label	I/O Type	Signal/Definition
		SERIAL INTERFACE
		In the DP/1, hardware interface circuits implement a CCITT V.24-compatible serial data interface with control signals provided through the DSP interface memory. In the DP/2, hardware circuits implement a V.24-compatible serial interface including control signals.
		The hardware interface signals are TTL compatible and can drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to RS-232-C voltage levels using 1489 receivers and 1488 drivers, or their equivalents. The serial interface timing is illustrated in Figure 2-6.
		In the DP/2, the $\overline{\text{RTS}}$ hardware control input is logically ORed with its corresponding interface memory bit by the modem to form the resultant control signal. The state of each hardware status output signal ($\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{RLSD}}$, and $\overline{\text{RI}}$) is also reflected in its corresponding interface memory bit. The hardware interface signals are complemented with respect to their corresponding interface memory bits (e.g., $\overline{\text{RTS}}$ signal low = RTS bit set to a 1).
TXD	IA	**Transmitted Data.** The modem obtains serial data to be transmitted from the host on the Transmitted Data (TXD) input in serial mode, or from the interface memory Transmit Data Register (TBUFFER) in parallel mode. (The TPDM bit selects serial or parallel mode.)
RXD	OA	**Received Data.** The modem presents received serial data to the host on the Received Data (RXD) output and to the interface memory Receive Data Register (RBUFFER) in both serial and parallel modes. RXD is clamped to mark in SDLC mode.
TDCLK	OA	**Transmit Data Clock.** In synchronous communication modes, the modem outputs a Transmit Data Clock (TDCLK). The TDCLK clock frequency is data rate ±0.01% with a duty cycle of 50 ± 1%. Transmit Data (TXD) must be stable during the one microsecond period immediately preceding and following the rising edge of TDCLK.
		In asynchronous modes, TDCLK is clamped to mark.
XTCLK	IA	**External Transmit Clock.** In synchronous communication modes, the host may supply the external transmit data clock input (XTCLK). The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is reflected at TDCLK if the modem is set for external clock (TXCLK bits = 11).
$\overline{\text{RDCLK}}$	OA	**Receive Data Clock.** In synchronous communication modes, the modem outputs a Receive Data Clock ($\overline{\text{RDCLK}}$) in the form of 50 ±1% duty cycle square wave. The low-to-high transitions of this output coincide with the center of received data bits.
		In asynchronous modes, $\overline{\text{RDCLK}}$ is clamped to mark.
$\overline{\text{RI}}$	OB	**Ring Indicator.** $\overline{\text{RI}}$ output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The OFF (high) condition of the $\overline{\text{RI}}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received.
		The $\overline{\text{RI}}$ frequency range is programmable in DSP RAM. $\overline{\text{RI}}$ will respond to RD input signals in the frequency range of 15.3 Hz to 68 Hz (default values).
		The $\overline{\text{RI}}$ OFF-to-ON (ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal on the RD input and the subsequent ON (OFF) transition of RI. The $\overline{\text{RI}}$ OFF-to-ON and ON-to-OFF transition response time is one period of the ring frequency.
$\overline{\text{RTS}}$	IA	**Request To Send (DP/2 Only).** $\overline{\text{RTS}}$ input ON (low) causes the modem to transmit data on TXD when $\overline{\text{CTS}}$ becomes active.
$\overline{\text{CTS}}$	OA	**Clear To Send (DP/2 Only).** $\overline{\text{CTS}}$ output ON (low) indicates that the modem will transmit any data present on TXD. Hardware signal $\overline{\text{CTS}}$ follows the CTS bit in interface memory by up to 4 baud in synchronous PSK modes. CTS response times relative to RTS are shown in Table 1-3.

**Table 2-7. Hardware Interface Signal Definitions (Cont'd)**

Label	I/O Type	Signal/Definition
		SERIAL INTERFACE (CONT'D)
DSR	OA	**Data Set Ready (DP/2 Only).** DSR output turns ON (low) to indicate the start of a training sequence.
RLSD	OA	**Received Line Signal Detector (DP/2 Only).** RLSD ON (low) indicates that valid data is available on RXD. The RLSD thresholds are programmable in DSP RAM. The RLSD default threshold values for both high and low channels are RLSD ON ≥ –43 dBm and RLSD OFF ≤ –48 dBm, respectively.
		DAA INTERFACE
RXA	DE	**Receive Analog.** RXA is an input to the external filter components from a data access arrangement (see Figure 8-1). The input impedance at RXA is determined by R13 (see Section 8). R13 is selected such that power at REC OUT is –9 dBm when the maximum signal is applied to RXA.
TXA	DF	**Transmit Analog.** The TXA output from the external filter components (see Figure 8-1) can drive a data access arrangement for connection to either the PSTN or a leased line. The transmitter output impedance is a 1458 type operational amplifier output. The maximum output level is determined by R15 (see Section 8).
		DAA INTERFACE SIGNALS
OHRELAY	OD	**Off-Hook Relay Driver.** OHRELAY is an open drain output which can drive a normally open relay with greater than 360 Ω coil resistance. OHRELAY ON closes the Off-Hook relay and connects the modem to the telephone line (off-hook). The OHRELAY output is controlled by the state of the RA bit, except in pulse dial mode. OHRELAY output is clamped off during power-on reset. An external discrete diode is not required across the relay coil.
RD	IA	**Ring Detect.** RD indicates to the modem by an ON (high) condition that a ringing signal is present. The signal (a 4N35 optoisolator compatible output) into the RD input should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40 Vrms, 15 Hz to 68 Hz, appearing across TIP and RING with respect to ground. The ring is then reflected on RI and the RI bit.
		ANCILLARY SIGNALS
T/DRC	IA	**Talk/Data Relay Control.** T/DRC is an uncommitted input that controls the state of the TLKRELAY output. T/DRC low turns the TLKRELAY output ON; T/DRC high turns the TLKRELAY output OFF.
TLKRELAY	OD	**Talk/Data Relay Driver.** TLKRELAY is an open drain output which can drive a normally closed relay with greater than 360 Ω coil resistance. The TLKRELAY output is controlled by the T/DRC input. The TLKRELAY output is clamped off during power-on reset. An external discrete diode is not required across the relay coil. In a typical application, TLKRELAY OFF opens the Talk/Data relay and disconnects the handset from the telephone line (i.e., the modem has control of the line.)
TBCLK, RBCLK	OA	**Transmitter Baud Clock and Receiver Baud Clock (DP/2 Only).** TBCLK and RBCLK outputs are provided in synchronous communication modes. TBCLK and RBCLK have no counterpart in the V.24 or RS-232-C recommendations since they mark the baud interval rather than the data rate for the transmitter and receiver, respectively. Both signals are active high. The high-to-low transition of each baud clock coincides with a high-to-low transition of the respective data clock. TBCLK and RBCLK are at 300 Hz for 1200 bps synchronous mode and 150 Hz for 600 bps synchronous mode, which is not the baud rate.

Table 2-7. Hardware Interface Signal Definitions (Cont'd)

		DIAGNOSTIC SIGNALS
		Four signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified. Timing of these signals is illustrated in Figure 2-7.
EYEX, EYEY	OB	**Eye Pattern Data X and Eye Pattern Data Y.** The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope horizontal (X) axis and vertical (Y) axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters.
		EYEX and EYEY outputs are 8-bit words, shifted out most significant bit first. EYEX and EYEY are clocked by the rising edge of EYECLK.
EYECLK	OA	**Eye Pattern Clock.** EYECLK is a clock for use by the serial-to-parallel converters. The EYECLK output is a 7200 Hz clock.
EYESYNC	OB	**Eye Pattern Sync.** EYESYNC is a strobe for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

Table 2-8. Microprocessor Bus Interface Timing

Parameter	Symbol	Min.	Max.	Units
CS Setup Time	TCS	0	–	ns
RSi Setup Time	TRS	25	–	ns
Data Access Time	TDA	–	75	ns
Data Hold Time	TDHR	10	–	ns
Control Hold Time	THC	10	–	ns
Write Data Setup Time	TWDS	20	–	ns
Write Data Hold Time	TDHW	10	–	ns
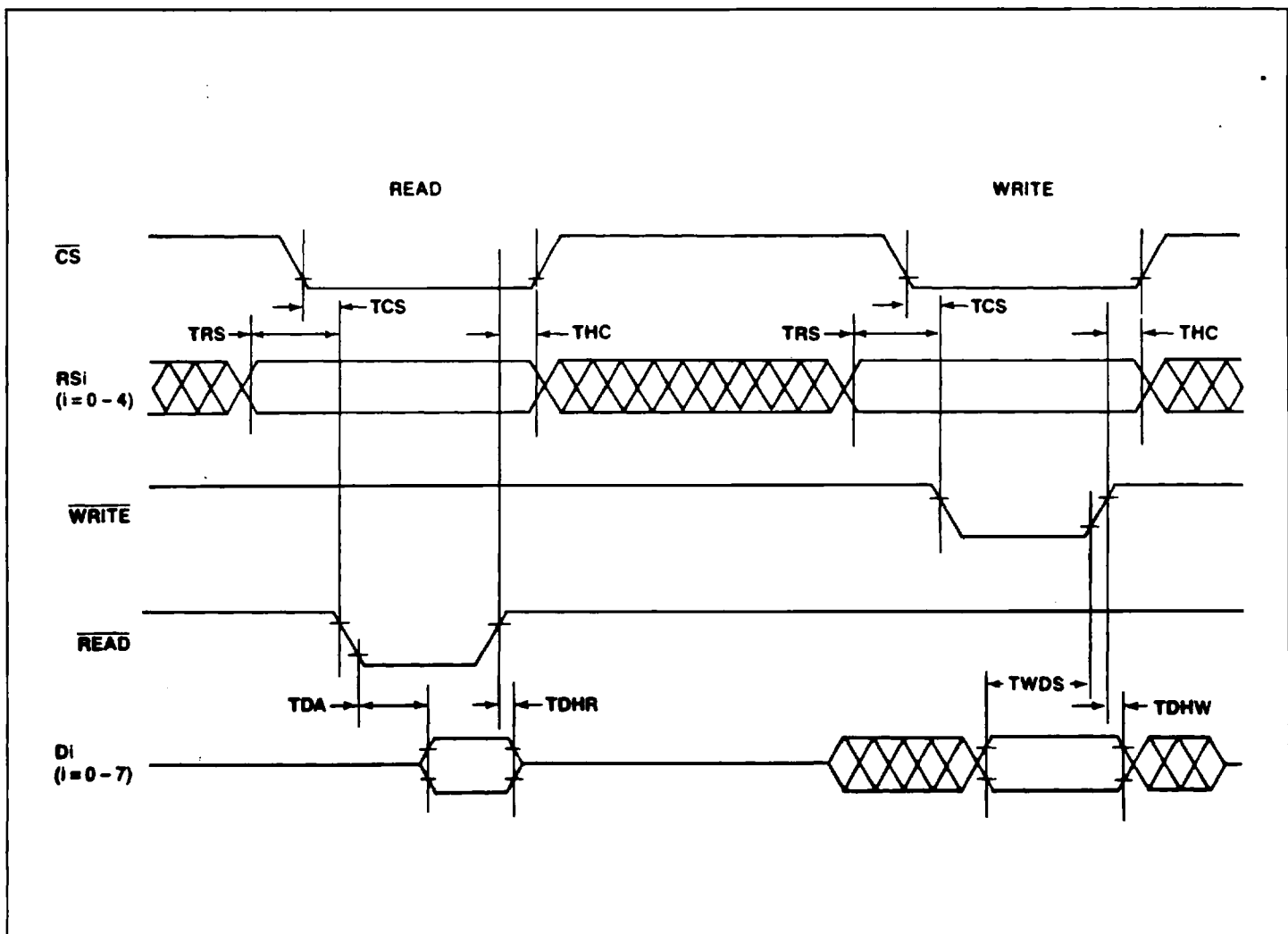
Figure 2-5. Microprocessor Bus Interface Waveforms
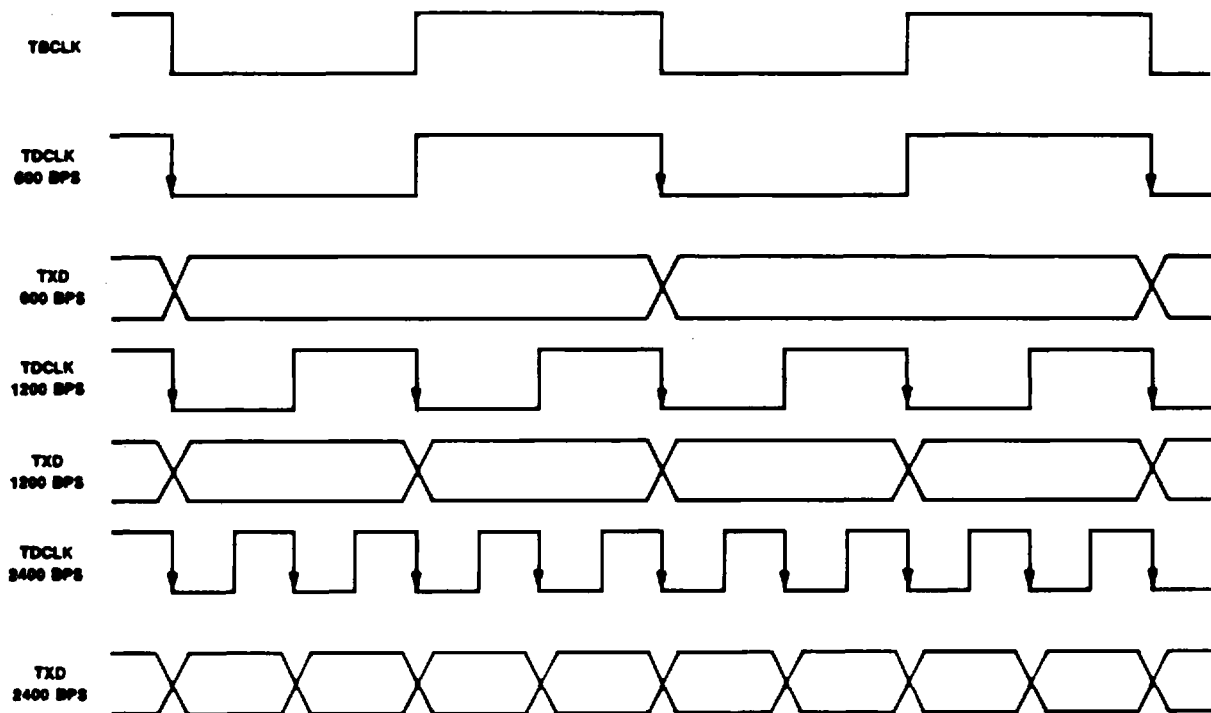
NOTE: THIS FIGURE IS VALID FOR SYNCHRONOUS MODE ONLY. THERE IS NO RELATIONSHIP BETWEEN TXD AND TDCLK IN ASYNCHRONOUS MODE

a. Transmit
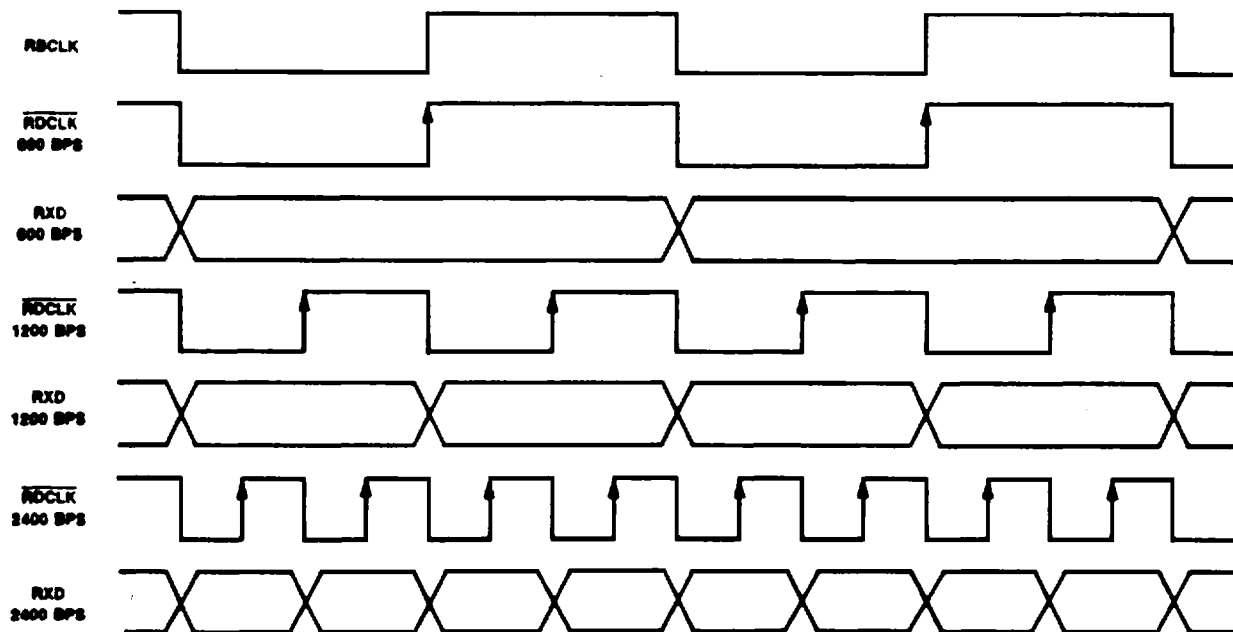
NOTE: THIS FIGURE IS VALID FOR SYNCHRONOUS MODE ONLY. THERE IS NO RELATIONSHIP BETWEEN RXD AND RDCLK IN ASYNCHRONOUS MODE

b. Receive

Figure 2-6. Serial Interface Waveforms
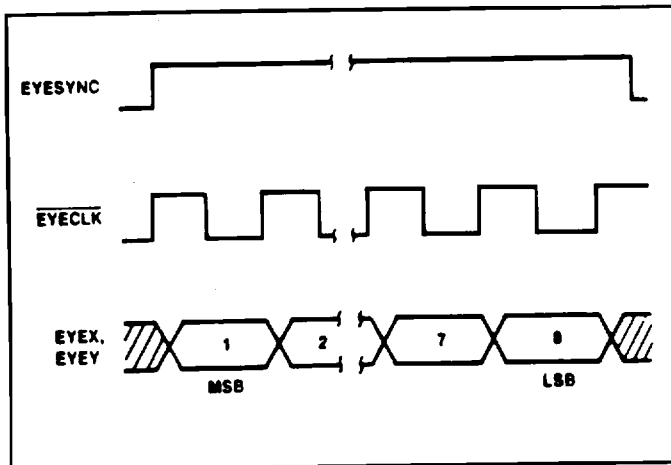
Figure 2-7. Eye Pattern Timing

3. SOFTWARE INTERFACE

3.1 INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

3.1.1 INTERFACE MEMORY MAP

A memory map of DSP interface memory identifying the contents of the 32 addressable registers is shown in Figure 3-1. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or group of bits in a register, the host processor must read a register then mask out unwanted data. When writ-

ing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, the host must read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory register.

3.1.2 INTERFACE MEMORY BIT DEFINITIONS

Table 3-1 defines the individual bits in the interface memory. Bits in the interface memory are referred to using the format Z:Q. The register number is denoted by Z (00 through 1F) and the bit number is located by Q (0 through 7, where 0 = LSB).

3.1.3 INITIALIZATION

The POR default value for each configuration/control bit is shown in Table 3-1. POR leaves the modem configured as follows:

- 2400 bps
- Synchronous
- Constant carrier
- Serial data mode
- Answer mode

Register	Bit 7	6	5	4	3	2	1	0
1F	NSIA	NCIA	—	NSIE	NEWS	NCIE	—	NEWC
1E	TDBIA	RDBIA	TDBIE	—	TDBE	RDBIE	—	RDBF
1D	XACC	XACK	—	—	—	—	XWT	XCR
1C	X RAM ADDRESS (XADD)							
1B	YACC	YACK	—	—	—	—	YWT	YCR
1A	Y RAM ADDRESS (YADD)							
19	X RAM DATA MSB (XDAM)							
18	X RAM DATA LSB (XDAL)							
17	Y RAM DATA MSB (YDAM)							
16	Y RAM DATA LSB (YDAL)							
15	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	—	—
13	TLVL			—	—	TXCLK		
12	CONFIGURATION (CONF)							
11	—	—	—	—	—	—	—	TXP
10	TRANSMIT DATA BUFFER (TBUFFER)							
0F	RLSD	—	CTS	DSR	RI	TM	SYNCD	FLAGS
0E	RTDET	BRKD	PE	FE	OE	SPEED		
0D	—	—	S1DET	SCR1	U1DET	SADET	—	—
0C	—	—	—	—	—	—	—	—
0B	TONEA	TONEB	TONEC	ATV25	ATBELL	—	—	BEL103
0A	—	—	—	—	—	—	—	CRCS
09	NV25	CC	DTMF	ORG	LL	DATA	PXQSEL	—
08	ASYNC	TPDM	—	DDIS	TRFZ	—	RTRN	RTS
07	RDLE	RDL	L2ACT	—	L3ACT	—	RA	MHLD
06	BRKS	EXOS	PARSL		PEN	STB	WDSZ	
05	—	—	—	—	CEQ	—	—	—
04	EQRES	—	—	—	EQFZ	IFIX	—	CRFZ
03	SYNCMD		SPLIT	—	ARC	SDIS	GTE	GTS
02	—	—	—	—	—	—	—	—
01	—	—	—	—	—	—	—	RXP
00	RECEIVER DATA BUFFER (RBUFFER)							
(—) indicates reserved for modem use only								

Figure 3-1. Interface Memory Map

Table 3-1. Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
ARC	03:3	0	**Automatic Rate Change Enable.** When control bit ARC is a 1, an automatic on-line rate change sequence is enabled. This allows on-line fallback from 2400 bps to 1200 bps per V.22 bis Section 6.6.
ASYNC	08:7	0	**Asynchronous/Synchronous.** When control bit ASYNC is a 1, asynchronous data mode is selected. When ASYNC changes from a 0 to a 1, the receiver's synchronous to asynchronous converter and the transmitter's asynchronous to synchronous converter are configured according to the EXOS, PARSL, PEN, STB and WDSZ bits at that time. ASYNC may be used to switch between synchronous and asynchronous modes at any time in idle or data mode. All clocks are clamped to mark in asynchronous mode.
			If an ASYNC connection is made immediately after POR, the host should write the value $000F to YRAM address $4A (YCR = 1) after selecting ASYNC = 1 in order to properly initialize the transmitter. ("C" code only)
			When ASYNC is a 0, synchronous data mode is selected. The SYNCMD bits further select one of two synchronous modes.
ATBELL	0B:3	0	**Bell Answer Tone Detected.** When set to a 1, status bit ATBELL indicates that the modem is detecting a 2225 Hz answer tone. When reset to a 0, the 2225 Hz answer tone is not being detected. ATBELL is active only in the Dial/Call Progress and originate handshake configurations.
ATV25	0B:4	0	**V25 Answer Tone Detected.** When set to a 1, status bit ATV25 signifies that the modem is detecting a 2100 Hz answer tone. When reset to a 0, the 2100 Hz answer tone is not being detected. ATV25 is only active in the Dial/Call Progress and certain originate handshake modes (ORG = 1), depending on the value of NV25.
BEL103	0B:0	0	**Bell 103 Mark Frequency Detected.** When set to a 1, status bit BEL103 indicates that the modem is detecting a Bell 103 mark frequency (1270 Hz). When reset to a 0, the mark frequency is not being detected. BEL103 is available only in Dial/Call Progress and answer handshake modes (ORG = 0).
BRKD	0E:6	0	**Break Detected.** When set to a 1, status bit BRKD indicates the modem is receiving continuous space. When reset to a 0, continuous space is not being received.
BRKS	06:7	0	**Break Sequence.** When control bit BRKS is a 1 in parallel asynchronous mode, the modem will send continuous space. When BRKS is a 0, the modem will transmit parallel data from the TBUFFER. (This bit is valid only when TPDM = 1.)
CC	09:6	0	**Controlled Carrier.** When control bit CC is a 1, the modem operates in controlled carrier (i.e., the carrier is controlled by RTS); when 0, the modem operates in constant carrier (i.e., the carrier stays on when RTS is off). Controlled Carrier is available only in leased line mode (LL = 1). Controlled carrier is not allowed in the V.23 configuration.
			Controlled carrier allows the modem transmitter to be controlled by the RTS pin or the RTS bit (see Table 1-3). When the RTS pin goes low, or the RTS bit set to a 1, the transmitter immediately sends scrambled ones for 270 ms and then turns on the CTS signal and the CTS bit. At 2400 bps, it is recommended that a retrain be sent once in the data mode to ensure that synchronization occurs. (V.22 bis)
			RTS should be ON when controlled carrier mode is selected.
			In PSK and QAM leased line, controlled carrier mode, the RTS delay between ON-to-OFF transition and OFF-to-ON transition must be equal to or greater than 50 ms.
CEQ	05:3	1	**Compromise Equalizer Enable.** When control bit CEQ is a 1, the transmitter's passband digital compromise equalizer is inserted into the transmit path. When CEQ is a 0, the equalizer is not inserted into the transmit path.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
CONF	12:0-7	84	**Modem Configuration Select.** The CONF control bits select the modem operating mode from one of the following configuration codes:

<table>
<tr><td></td><td></td><td colspan="2">Data Rate (bps)</td><td>CONF</td><td></td></tr>
<tr><td></td><td>Mode</td><td>Transmit</td><td>Receive</td><td>(Hex)</td><td>Notes</td></tr>
<tr><td></td><td>V.22 bis</td><td>2400</td><td>2400</td><td>84</td><td>2, 6</td></tr>
<tr><td></td><td>V.22</td><td>1200</td><td>1200</td><td>52</td><td></td></tr>
<tr><td></td><td>V.22</td><td>600</td><td>600</td><td>51</td><td>3</td></tr>
<tr><td></td><td>Bell 212A</td><td>1200</td><td>1200</td><td>62</td><td></td></tr>
<tr><td></td><td>Bell 103</td><td>0-300</td><td>0-300</td><td>60</td><td>4</td></tr>
<tr><td></td><td>V.21</td><td>300</td><td>300</td><td>A0</td><td>4</td></tr>
<tr><td></td><td>V.23</td><td>75</td><td>1200</td><td>46</td><td>4, 5, 7, 8</td></tr>
<tr><td></td><td>V.23</td><td>1200</td><td>75</td><td>47</td><td>4, 7</td></tr>
<tr><td></td><td>V.23</td><td>1200</td><td>1200</td><td>42</td><td>4, 7, 8</td></tr>
<tr><td></td><td>V.23</td><td>75</td><td>75</td><td>40</td><td>4, 7</td></tr>
<tr><td></td><td>Tone Generator/Detector</td><td></td><td></td><td>80</td><td></td></tr>
<tr><td></td><td>Dial/Call Progress Monitor</td><td></td><td></td><td>81</td><td></td></tr>
</table>

Notes:

1. The host must set NEWC to a 1 after changing CONF.

2. The modem supports automatic rate detection between V.22, V.22 bis, and Bell 212 configurations. To allow the modem to transmit according to the negotiated data rate after a handshake, the host should update CONF and set the NEWC bit after determining the line speed (see SPEED). (See Section 7 to implement a more comprehensive rate detection/reconfiguration scheme.)

3. In V.22 (600 bps) configuration, the host must toggle the DATA bit (and set NEWC each time) after RLSD turns ON following a line hit.

4. When making a connection in any FSK mode with noise present above the threshold, the host should follow the procedure shown in Figure 3-2 to prevent false detection of carrier. After the call is disconnected, the host should restore the default value of $2500 into the Max AGC Gain Word (XRAM address $3F, XCR = 0). (See Section 3.3.)

5. In V.23 75Tx/1200Rx configuration, the host must initialize the AGC Gain Slew Rate (YRAM address $12, YCR = 0) with value $0200 (RC2324DP "C" code only).

6. When reconfiguring from any FSK mode to V.22 bis synchronous mode, the host should change configuration with ASYNC = 1 before setting ASYNC = 0 in order to correctly initialize the transmitter.

7. RC2324DP only.

8. RLSD ON-to-OFF time is 29.5 ms rather than the recommended 5-15 ms.

Mnemonic	Memory Location	Default Value	Name/Description
CRCS	0A:0	0	**CRC Sending.** When set to a 1, status bit CRCS indicates that the transmitter is sending the CRC (2 bytes) in SDLC/HDLC mode. A 0 indicates that the CRC is not being sent.
CRFZ	04:0	0	**Carrier Recovery Freeze.** When control bit CRFZ is a 1, updating of the receiver's carrier recovery phase lock loop (PLL) is inhibited. When reset to a 0, normal updating is enabled.
CTS	0F:5	0	**Clear to Send.** When set to a 1, status bit CTS indicates that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted (see TPDM). CTS response times from an RTS ON or OFF transition after the modem has completed a handshake are shown in Table 1-3. When reset to a 0, data is not being transmitted.
			CTS is independent of RTS when in analog loopback mode, and after exiting digital loopback mode or retrain. Since the host controls the CTS signal to the DTE, the host must set/reset the CTS bit conditioned upon the DTE RTS signal.
DATA	09:2	0	**Data Mode.** When control bit DATA is a 0, the modem is in the idle mode and data is not being transmitted. The modem is prevented from entering and proceeding with the handshake (start-up) sequence and will ignore all V.24 interface signals. This bit should be set to a 1 by the host at a suitable time after completion of dialing or answering.
			When control bit DATA is a 1, the modem is in the data mode in either leased line mode (LL = 1) or handshake mode (LL = 0).

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
DDIS	08:4	0	**Descrambler Disable.** When control bit DDIS is a 1, the receiver's descrambler circuit is disabled; when a 0, the descrambler circuit is enabled.
DSR	0F:4	0	**Data Set Ready.** Status bit DSR is set to a 1 at the start of a training sequence.
DTMF	09:5	0	**DTMF Select.** When the modem is configured for dialing mode (CONF = 81), the modem will dial using DTMF tones or pulses. When control bit DTMF is a 1, the modem will dial using DTMF tones. When DTMF is a 0, the modem will dial using pulses. The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. When in dialing mode, the data placed in the Transmitter Data Buffer (TBUFFER) is treated as the digit to be dialed. The number to be dialed must be represented by two hexadecimal digits (e.g., if a 9 is to be dialed, then a 09 must be written to the TBUFFER). (See TDBE.)
			Dialing timing is host programmable in DSP RAM.
EQFZ	04:3	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited. When a 0, updating is enabled.
EQRES	04:7	0	**Equalizer Reset.** When control bit EQRES is a 1, the receiver adaptive equalizer taps are reset to zero. When a 0, the equalizer taps are updated normally.
EXOS	06:6	0	**Extended Overspeed.** When control bit EXOS is a 1, Extended Overspeed mode is selected in the transmitter async-to-sync converter and in the receiver sync-to-async converter. When a 0, normal overspeed mode is selected. (See SPLIT)
FE	0E:4	0	**Framing Error.** When set to a 1, status bit FE indicates that more than 1 in 8 (or 1 in 4 for extended overspeed) characters were received without a Stop bit in asynchronous mode or an ABORT sequence was detected in SDLC/HDLC synchronous mode. When reset to a 0, no framing error is detected.
FLAGS	0F:0	0	**Flag Sequence.** When set to a 1, status bit FLAGS indicates that the transmitter is sending the Flag sequence in SDLC/HDLC mode, or a constant mark in parallel asynchronous mode. When reset to a 0, FLAGS indicates that the transmitter is sending data.
GTE	03:1	0	**Guard Tone Enable.** When control bit GTE is a 1, the specified guard tone to be transmitted is enabled according to the state of the GTS bit (CCITT configurations only). The guard tone will be transmitted only by the answering modem. When set to a 0, guard tone transmission is disabled. (V.22 bis)
GTS	03:0	0	**Guard Tone Select.** When control bit GTS is set to a 1, the 550 Hz tone is selected; when a 0, the 1800 Hz tone is selected. The selected guard tone will be transmitted only when GTE is enabled. (V.22 bis)
IFIX	04:2	1	**Eye Fix.** When control bit IFIX is a 1, the serial diagnostic data output on the EYEX and EYEY pins reflects the Rotated Equalizer Output. When IFIX is a 0, the data on EYEX and EYEY is selected by the addresses in X RAM Address and Y RAM Address registers, respectively.
LL	09:3	0	**Leased Line.** When control bit LL is set to a 1, the modem will enter the leased line data mode when the DATA bit is a 1. When a 0, the modem will enter the Handshake Mode when the DATA bit is a 1.
			The host should select the leased line mode by setting the LL bit (and the NEWC bit) after handshake is completed in switched line mode. This sequence allows incorporation of a carrier recovery algorithm in the leased line mode.
L2ACT	07:5	0	**Loop 2 (Local Digital Loopback) Activate.** When control bit L2ACT is a 1, the receiver's digital output is internally connected to the transmitter's digital input (locally activated digital loopback) in accordance with CCITT Recommendation V.54.

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Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
L3ACT	07:3	0	**Loop 3 (Local Analog Loopback) Activate.** When control bit L3ACT is a 1, the transmitter's analog output is internally coupled to the receiver's analog input (local analog loopback) in accordance with CCITT Recommendation V.54. The modem may only be placed into loop 3 mode when in idle mode (DATA bit is a 0). After setting the L3ACT bit to a 1, the NEWC bit must also be set. The loopback is then completed when the modem sets DSR, CTS, and DCD (RLSD) bits to a 1. To terminate the loopback, reset L3ACT to a 0 and then set NEWC to a 1.
MHLD	07:0	0	**Mark Hold.** When control bit MHLD is a 1, the transmitter sends continuous mark. When MHLD is a 0, the transmitter sends continuous flag or data from TBUFFER. This bit is valid only in SDLC/HDLC mode.
NCIA	1F:6	0	**NEWC Interrupt Active.** When the new configuration interrupt is enabled (NCIE is a 1) and a new configuration is implemented (NEWC is reset to a 0 by the DSP), IRQ is asserted and status bit NCIA is set to a 1 to indicate that NEWC being a 0 caused the interrupt. NCIA and the interrupt request due to NEWC are cleared by the host writing a 0 into NCIE. (See NEWC and NCIE.)
NCIE	1F:2	0	**NEWC Interrupt Enable.** When control bit NCIE is a 1 (interrupt enabled), the modem will assert IRQ and set NCIA to a 1 when the NEWC bit is reset to a 0 by the DSP. When NCIE is a 0 (interrupt disabled), NEWC has no effect on IRQ or NCIA. (See NEWC and NCIA.)
NEWC	1F:0	0	**New Configuration.** When control bit NEWC is set to a 1, the modem will implement the new configuration. The DSP resets the NEWC bit to a 0 when the configuration change is acknowledged. A configuration change can also cause IRQ to be asserted. (See NCIE and NCIA.) **Note:** Control bit NEWC must be set to a 1 by the host after the host changes the contents of any of the following control bits: ASYNC — Asynchronous Mode CONF — Configuration DATA — Data EQRES — Equalizer Reset GTE — Guard Tone Enable GTS — Guard Tone Select L2ACT — Loop 2 Activate L3ACT — Loop 3 Activate LL — Leased Line Mode ORG — Originate Mode PARSL — Parity Select PEN — Parity Enable RA — Relay Activate RDL — Remote Digital Loopback Request RDLE — Remote Digital Loopback Enable RTRN — Retrain STB — Stop Bit Number SYNCMD — Synchronous Mode Select TLVL — Transmit Level WDSZ — Word Size
NEWS	1F:3	–	**New Status.** When set to a 1, status bit NEWS indicates that one or more status bits located in registers 0A, 0B, 0E, or 0F have changed state, or a DSP RAM read or write has been completed. This bit can be reset to a 0 only by the host. When set to a 1, this bit can cause IRQ to be asserted. (See NSIE and NSIA.)
NSIA	1F:7	0	**NEWS Interrupt Active.** When the new status interrupt is enabled (NSIE is a 1) and a change of status occurs (NEWS is set to a 1), IRQ is asserted and status bit NSIA is set to a 1 to indicate that NEWS being a 1 caused the interrupt. NSIA and the interrupt request due to NEWS are cleared when the host writes a 0 to NEWS. (See NEWS and NSIE.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
NSIE	1F:4	0	**NEWS Interrupt Enable.** When control bit NSIE is a 1 (interrupt enabled), IRQ will be asserted and NSIA will be set to a 1 when NEWS is set to a 1 by the DSP. When NSIE is a 0 (interrupt disabled), NEWS has no effect on IRQ or NSIA. (See NEWS and NSIA.)
NV25	09:7	0	**No. V.25 Answer Tone.** When the modem is in answer mode and control bit NV25 is set to a 1, the transmitter will not transmit the 2100 Hz CCITT answer tone when a handshake sequence is initiated. This bit should not be set if the modem is configured for Bell 212 answer mode. NV25 should always be set if the modem is configured for Bell 103 answer mode. When the modem is in PSK originate mode and NV25 = 1, the modem will not be affected. When the modem is in FSK originate mode and NV25 = 1, status bit ATV25 will not reflect that the 2100 Hz answer tone is being received. NV25 should not be set if the modem is configured for Bell 103 originate mode. When NV25 is reset to a 0, the modem will transmit the answer tone in answer mode and will detect answer tone in originate mode.
OE	0E:3	0	**Overrun Error.** When set to a 1, status bit OE indicates that the Receiver Data Buffer (RBUFFER) was loaded from the RXA input before the host read the old data from RBUFFER. When reset to a 0, RBUFFER was read before new receive data was loaded into RBUFFER. This is valid for both ASYNC mode and SDLC/HDLC mode.
ORG	09:4	0	**Originate.** When control bit ORG is a 1, the modem is in originate mode; when a 0, the modem is in answer mode. **Note:** The NEWC bit must be set after the ORG bit is changed.
PARSL	06:4, 5		**Parity Select.** Control bits PARSL select the method by which parity is generated and checked during the asynchronous parallel data mode (ASYNC = 1). The options are: 5 4 **Parity Selected** 0 0 Stuff Parity ("9th Data Bit") (see TXP, RXP) 0 1 Space Parity 1 0 Even Parity 1 1 Odd Parity
PE	0E:5	0	**Parity Error.** When set to a 1, status bit PE indicates that a character with bad parity was received in the asynchronous mode, or bad CRC was detected in the SDLC/HDLC synchronous mode. When a 0, a character with good parity was received.
PEN	06:3	0	**Parity Enable.** When set to a 1, control bit PEN enables parity generation and checking during asynchronous parallel data mode. When reset to a 0, parity generation and checking is disabled.
PKGSEL	09:1	0	**Package Select.** When set to a 1, control bit PKGSEL indicates that the single device implementation is selected. **NOTE: This bit must be set to a 1 upon power-on-reset processing.** (RC2324DP/1 and RC2424DP/1 only)
RA	07:1	0	**Off-Hook Relay Activate.** When control bit RA is set to a 1, the OHRELAY output is activated causing the relay to close (off-hook); when RA is reset to 0, the OHRELAY is turned off causing the relay to open (on-hook). **Note:** The host has exclusive control of the OHRELAY output through the RA bit except in pulse dial mode.
RBUFFER	00:0-7	0	**Receive Data Buffer.** The host obtains data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER.
RDBF	1E:0	–	**Receiver Data Buffer Full.** When set to a 1, status bit RDBF signifies that the modem wrote valid received data into register 00 (RBUFFER). This condition can also cause IRQ to be asserted. The host reading or writing register 00 resets the RDBF bit to 0. (See RDBIE and RDBIA.)
RDBIA	1E:6	0	**Receiver Data Buffer Interrupt Active.** When the receiver data buffer full interrupt is enabled (RDBIE is a 1) and register 00 is written to by the DSP (RDBF is set to a 1), the modem asserts IRQ and sets RDBIA to a 1 to indicate that RDBF being a 1 caused the interrupt. The host reading or writing register 00 resets the RDBF bit to a 0 and clears the interrupt request due to RDBF. (See RDBF and RDBIE.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
RDBIE	1E:2	0	**Receiver Data Buffer Interrupt Enable.** When control bit RDBIE is a 1 (interrupt enabled), the modem will assert IRQ and set the RDBIA bit to a 1 when RDBF is set to a 1 by the DSP. When RDBIE is a 0 (interrupt disabled), RDBF has no effect on IRQ or RDBIA. (See RDBF and RDBIA.)
RDL	07:6	0	**Remote Digital Loopback Request.** When control bit RDL is a 1, the modem initiates a request for the remote modem to go into digital loopback, RXD is clamped to a mark, and the RLSD bit and RLSD signal will be reset until the loop is established. When the host resets the RDL bit the modem sends the RDL terminating sequence. Figure 3-3 illustrates remote digital loopback timing.
			If a remote digital loopback request is initiated at the same time a retrain is requested from the remote modem, the modem will remain in an indefinite state waiting for the request to be acknowledged. In order to exit from this condition, the procedure shown in Figure 3-4 should be followed.
RDLE	07:7	0	**Remote Digital Loopback Response Enable.** When set to a 1, control bit RDLE enables the modem to respond to the remote modem's digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to a mark; resets the CTS and RLSD bits to a 0, and turns the CTS and DCD signals OFF. The TM bit is set to a 1 to inform the host of the test status.
			The RDLE bit should only be set while the modem is in Idle mode (DATA = 0)
RI	0F:3	0	**Ring Indicator.** When set to a 1, status bit RI indicates that a valid ringing signal is being detected. Ringing is detected if pulses are present on the RD input in the 15 Hz - 68 Hz frequency range (default frequency range). The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time coincident with RI output signal. The minimum and maximum valid ring frequencies are host programmable in DSP RAM. If the maximum value is set to zero, the RI bit will go on and off with each half of the ring frequency sine wave.
RLSD	0F:7	0	**Received Line Signal Detector.** When status bit RLSD is set to a 1, the carrier is being detected and receive data is valid. When a 0, the carrier is not being detected and RXD output is clamped to mark. **Note:** RXD is also clamped to mark during retrain while the RLSD bit remains on.
			In V.23 controlled carrier mode, if RTS is turned OFF, RLSD is turned OFF momentarily from 400 ms to 1 second depending on whether the modem is receiving in the main or back channel (RC2324DP only).
RTDET	0E:7	0	**Retrain Detected.** When set to a 1, status bit RTDET indicates that a retrain request sequence has been detected.
RTRN	08:1	0	**Retrain.** When control bit RTRN set to a 1 and the modem is in data mode, the modem requests retrain (or automatic rate change - see ARC) from the remote modem. RTRN is set to 0 when the previous retrain is completed. **Note:** If retrain is not completed successfully, the host must clear the RTRN bit.
			Fallback from 2400 bps to 1200 bps per CCITT V.22 bis may be accomplished as follows:
			1. Set the ARC bit to a 1 in both modems. 2. Set the RTRN bit to a 1 in either modem. 3. Set the NEWC bit to a 1.
			Fall forward from 1200 bps to 2400 may be accomplished as follows:
			1. Reset the ARC bit (with the remote modem having the ARC bit set). 2. Set the RTRN bit. 3. Set the NEWC bit.
			If the remote modem can operate at the requested rate, the SPEED bits will be changed by the modem to reflect the new rate after the retrain is completed.
			If a retrain request or retrain/fallback request is not acknowledged by the remote modem, the modem will remain in an indefinite state waiting for the request to be acknowledged. In order to exit this condition, the procedure shown in Figure 3-4 should be followed.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
RTS	08:0	0	**Request to Send.** Control bit RTS is set to a 1 to request the transmitter to send data.
RXP	01:0	0	**Received Parity bit.** This bit is only valid when parity is enabled (PEN = 1), and word size is set for 8 bits per character (WDSZ = 11). In this case, the parity bit received (or ninth data bit) will be available at this location. The host must read this bit before reading the received data buffer (RBUFFER).
S1DET	0D:5	0	**S1 Sequence Detected.** Status bit S1DET is set to a 1 when the S1 sequence is being detected. This bit is reset to a 0 when the S1 sequence is not being detected.
SADET	0D:2	0	**Scrambled Alternating Ones Sequence Detected.** Status bit SADET is set to a 1 when the Scrambled Alternating Ones sequence is being detected. This bit is reset to a 0 when the Scrambled Alternating Ones sequence is not being detected. **Note:** SADET is used to indicate the response of the remote modem to a V.22 bis rate change request or a remote digital loopback request.
SCR1	0D:4	0	**Scrambled Ones Sequence Detected.** Status bit SCR1 is set to a 1 when Scrambled Ones is being detected during handshake. This bit is reset to 0 when Scrambled Ones is not being detected.
SDIS	03:2	0	**Scrambler Disable.** When control bit SDIS is a 1, the transmitter scrambler is disabled; when SDIS is a 0, the scrambler is enabled.
SPEED	0E:0-2	0	**Speed Indication.** The SPEED status bits indicate the data rate at the completion of a handshake:

SPEED (continued):

2	1	0	Data Rate (bps)
0	0	0	Default
0	0	1	600
0	1	0	1200
0	1	1	2400

In leased line mode (LL = 1), the host must delay 300 ms after RLSD is set before reading the SPEED bits.

Mnemonic	Memory Location	Default Value	Name/Description
SPLIT	03:5	0	**Parallel Async Extended Overspeed TX/RX Split.** When SPLIT is set to a 1 and EXOS is set, the transmitter will transmit at the basic overspeed rate while the receiver receives at the extended overspeed rate.
STB	06:2	0	**Stop Bit Number.** When control bit STB is a 0, one stop bit is selected in asynchronous mode; when a 1, two stop bits are selected.
SYNCD	0F:1	0	**Sync Pattern Detected.** When set to a 1, status bit SYNCD indicates that SDLC/HDLC flags (7E pattern) are being detected. When reset to a 0, the 7E pattern is not being detected. This bit is valid only in SDLC/HDLC mode (SYNCMD = 01).
SYNCMD	03;6,7	0	**Synchronous Mode.** Configuration bits SYNCMD select the synchronous mode (ASYNC = 0) from the following:

SYNCMD (continued):

7	6	Synchronous Mode
0	0	Normal Sync
0	1	SDLC/HDLC Sync

Mnemonic	Memory Location	Default Value	Name/Description
TBUFFER	10:0-7	00	**Transmitter Data Buffer.** The host conveys output data to the transmitter in the parallel mode (TPDM = 1) by writing a data byte to the TBUFFER when the TDBE bit is a 1. Bit 0 of the data is transmitted first.
TDBE	1E:3	–	**Transmitter Data Buffer Empty.** When set to a 1, status bit TDBE signifies that the modem has read transmit data from register 10 (TBUFFER) and the host can write new data into register 10. This condition can also cause IRQ to be asserted. The host reading or writing register 10 resets the TDBE bit to 0. (See TDBIE and TDBIA.)

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Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
TDBIA	1E:7	0	**Transmitter Data Buffer Interrupt Active.** When the transmitter data buffer empty interrupt is enabled (TDBIE is a 1) and register 10 is empty (TDBE is set to a 1), the modem asserts IRQ and sets status bit TDBIA to a 1 to indicate that TDBE being a 1 caused the interrupt. Writing to register 10 or resetting TDBIE resets the TDBIA bit to a 0 and clears the interrupt request due to TDBE. (See TDBIE and TDBE.)
TDBIE	1E:5	0	**Transmitter Data Buffer Interrupt Enable.** When control bit TDBIE is a 1 (interrupt enabled), the modem will assert IRQ and set the TDBIA bit to a 1 when TDBE is set to 1 by the DSP. When TDBIE is a 0 (interrupt disabled), TDBE has no effect on IRQ or TDBIA. (See TDBE and TDBIA.)
TLVL	13:4-7	6	**Transmit Level Attenuation Select.** The TLVL control code selects the transmitter analog output level attenuation at the TXA pin as follows: 7 6 5 4 — Transmit Level Attenuation (dB ±0.5 dB) 0 0 0 0 — 0 dB 0 0 0 1 — 1 dB 0 0 1 0 — 2 dB 0 0 1 1 — 3 dB 0 1 0 0 — 4 dB 0 1 0 1 — 5 dB 0 1 1 0 — 6 dB 0 1 1 1 — 7 dB 1 0 0 0 — 8 dB 1 0 0 1 — 9 dB 1 0 1 0 — 10 dB 1 0 1 1 — 11 dB 1 1 0 0 — 12 dB 1 1 0 1 — 13 dB 1 1 1 0 — 14 dB 1 1 1 1 — 15 dB The host can fine tune the transmit level to a value lying within a 1 dB step by changing a value in DSP RAM.
TM	0F:2	0	**Test Mode.** When set to a 1, status bit TM indicates that the selected test mode is active. When TM is reset to a 0, no test mode is active.
TONEA	0B:7	0	**Tone Filter A Energy Detected.** When set to a 1, status bit TONEA indicates that energy above the threshold is being detected by the Call Progress Monitor filter in the Dial Configuration (CONF = 81) or that 1300 Hz FSK tone energy is being detected by the Tone A bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TONEB	0B:6	0	**Tone Filter B Energy Detected.** When set to a 1, status bit TONEB indicates that 390 Hz FSK tone energy is being detected by the Tone B bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TONEC	0B:5	0	**Tone Filter C Energy Detected.** When set to a 1, status bit TONEC indicates that either 1650 Hz (ORG = 1) or 980 Hz (ORG = 0) FSK tone energy is being detected by the Tone C bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TPDM	08:6	0	**Transmitter Parallel Data Mode.** When control bit TPDM is a 1, the transmitter accepts parallel data from the host microprocessor interface via the TBUFFER register for transmission rather than serial data from the TXD input pin. When TPDM is a 0, serial data from the TXD input pin is accepted for transmission rather than parallel data from TBUFFER.
TRFZ	08:3	0	**Timing Recovery Freeze.** When control bit TRFZ is a 1, the updating of the receiver's timing recovery algorithm is inhibited. When TRFZ is a 0, normal updating occurs.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
TXCLK	13:0,1	0	**Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock:
			1 0 **Transmit Clock**
			0 0 Internal
			0 1 Not Used (Internal)
			1 0 Slave (RDCLK output)
			1 1 External (XTCLK input)
			When the external clock is chosen, the host supplied clock must be connected to the XTCLK input pin. The external clock will then be reflected at the TDCLK output pin.
			When the slave clock is chosen, the transmitter clock output (TDCLK) is phase locked to the receiver clock output (RDCLK).
TXP	11:0	0	**Transmit Parity bit.** This bit is only active when parity is enabled (PEN = 1), stuff parity is selected (PARSL = 00) and word size is set for 8 bits per character. The host must load the stuffed parity bit (or ninth data bit) in this location before loading the other 8 bits of data in TBUFFER.
U1DET	0D:3	0	**Unscrambled Ones Detected.** When set to a 1, status bit U1DET indicates that Unscrambled Ones sequence has been detected. This bit is reset to a 0 by the modem at the end of the Unscrambled Ones sequence. (V.22 bis)
WDSZ	06:0,1	0	**Data Word Size.** The WDSZ control field sets the number of data bits per character in asynchronous mode as follows:
			1 0 **Data Bits/Character**
			0 0 5
			0 1 6
			1 0 7
			1 1 8
			The total number of bits/character depends on WDSZ, PEN, and STB bits.
XACC	1D:7	0	**X RAM Access Enable.** When control bit XACC is a 1, the DSP accesses the X RAM associated with the address in XADD and the XCR bit. XWT determines if a read or write is performed. The DSP resets XACC to a 0 upon RAM access completion.
XADD	1C:0-7	00	**X RAM Address.** XADD contains the X RAM address used to access the DSP's X Data RAM (XCR = 0) or X Coefficient RAM (XCR = 1) via the X RAM Data LSB and MSB registers (addresses 18 and 19, respectively). (See Table 3-2.)
XCR	1D:0	0	**X Coefficient RAM Select.** When control bit XCR is a 1, XADD applies to the X Coefficient RAM. When XCR is a 0, XADD applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 3-2).
XDAL	18:0-7	00	**X RAM Data LSB.** XDAL is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XDAM	19:0-7	00	**X RAM Data MSB.** XDAM is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XWT	1D:1	0	**X RAM Write.** When XWT is a 1 and XACC is set to a 1, the DSP copies data from the X RAM Data registers (18 and 19) into the X RAM location addressed by XADD and XCR. When control bit XWT is a 0 and XACC is set to a 1, DSP reads X RAM at the location addressed by XADD and XCR and stores the data into the X RAM Data registers (18 and 19).
YACC	1B:7	0	**Y RAM Access Enable.** When control bit YACC is a 1, the DSP accesses the Y RAM associated with the address in YADD and the YCR bit. YWT determines if a read or write is performed. The DSP resets YACC to a 0 upon RAM access completion.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
YADD	1A:0-7	00	**Y RAM Address.** YADD contains the Y RAM address used to access the DSP's Y Data RAM (YCR = 0) or Y Coefficient RAM (YCR = 1) via the Y RAM Data LSB and MSB registers (addresses 16 and 17, respectively). (See Table 3-2.)
YCR	1B:0	0	**Y Coefficient RAM Select.** When control bit YCR is a 1, YADD applies to the DSP's Y Coefficient RAM. When YCR is a 0, YADD applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 3-2).
YDAL	16:0-7	00	**Y RAM Data LSB.** YDAL is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YDAM	17:0-7	00	**Y RAM Data MSB.** YDAM is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YWT	1B:1	0	**Y RAM Write.** When YWT is a 1 and YACC is set to a 1, the DSP copies data from the Y RAM Data registers (16 and 17) into the Y RAM location addressed by YADD and YCR. When control bit YWT is a 0 and YACC is set to a 1, the DSP reads Y RAM at the location addressed by YADD and YCR and stores the data into the Y RAM Data registers (16 and 17).

```
        ┌──────────┐                      ┌──────────┐              ┌──────────────┐
        │  START   │                      │  START   │◄─────────────│  COLLECTING  │
        └────┬─────┘                      └────┬─────┘              │   AGC DATA   │
             │                                 │                    └──────────────┘
      ┌──────┴──────┐                   ┌──────┴──────┐
      │ 1 ─► DATA   │                   │ $3F ─► XADD │
      │   (09:2)    │                   │  (1C:0-7)   │
      └──────┬──────┘                   └──────┬──────┘
             │                                 │
      ┌──────┴──────┐                   ┌──────┴──────┐
      │ 1 ─► NEWC   │                   │ $81 ─► REG$1D│          (SET XACC, XCR)
      │    (1F:0)   │                   │             │
      └──────┬──────┘                   └──────┬──────┘
             │◄────────┐                       │◄────────┐
         ╱───┴───╲  NO │                   ╱───┴───╲  NO │
        ╱ NEWC = 0?╲───┘                  ╱ XACC = 0?╲───┘
        ╲         ╱                       ╲         ╱
         ╲───┬───╱                         ╲───┬───╱
             │ YES                             │ YES
      ┌──────┴───────────┐            ┌─────────┴────────┐
      │ COLLECT AT LEAST │            │ READ XDAM, XDAL  │
      │ 10 MILLISECONDS  │            │ TO OBTAIN MSB,   │
      │ OF AGC VALUES,   │            │ LSB              │
      │ SEE SUBROUTINE   │            │ (19:0-7, 18:0-7) │
      │ "COLLECTING AGC  │            └─────────┬────────┘
      │  DATA"           │                      │
      └──────┬───────────┘                      │
             │                                  │
      ┌──────┴──────┐                           │
      │ CALCULATE   │                           │
      │ AVERAGE AGC │                           │
      │ VALUE       │                           │
      └──────┬──────┘                           │
             │                                  │
      ┌──────┴───────────┐                      │
      │ CALCULATE MAX G  │                      │
      │ MAXG=[(6dB/      │                      │
      │ 0.097656dB)•64]  │                      │
      │ HEX + AVERAGE AGC│                      │
      └──────┬───────────┘                      │
             │                                  │
      ┌──────┴──────────┐                       │
      │ MSB (MAXG) ─► XDAM                       │
      │ (19:0-7)        │                       │
      │ LSB (MAXG) ─► XDAL                       │
      │ (18:0-7)        │                       │
      └──────┬──────────┘                       │
             │                                  │
      ┌──────┴──────┐                           │
      │ $3F ─► XADD │                           │
      │  (1C:0-7)   │                           │
      └──────┬──────┘                           │
             │                                  │
      ┌──────┴──────┐                           │
      │ $82 ─►      │                           │
      │ REGISTER 1D │                           │
      └──────┬──────┘                           │
             │◄────────┐                        │
         ╱───┴───╲  NO │                        │
        ╱ XACC = 0?╲───┘                        │
        ╲         ╱                             │
         ╲───┬───╱                              │
             │ YES                              │
        ┌────┴─────┐                       ┌────┴─────┐
        │   END    │                       │   END    │
        └──────────┘                       └──────────┘
```

Figure 3-2. FSK Connection with Noise Above Threshold
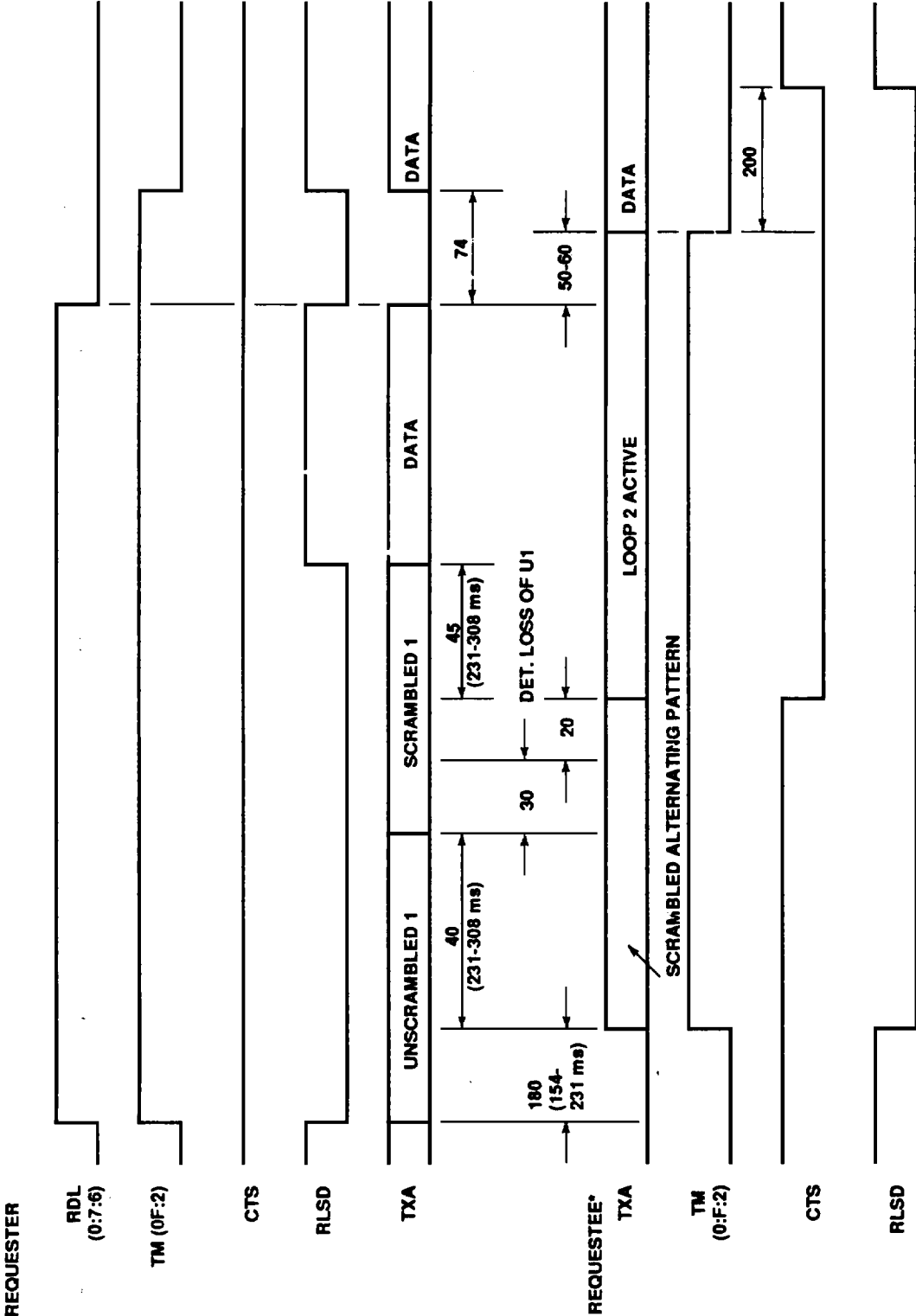
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Figure 3-3. V.22 bis Remote Digital Loopback Timing

```
                    ╱╲
                   ╱    ╲
                  ╱ RTRN/ARC/RDL ╲        NO
                 ╱ NOT ACKNOWLEDGED ╲────────────┐
                 ╲ (TIMEOUT CLOCK  ╱             │
                  ╲  EXPIRED)    ╱               │
                   ╲          ╱                  │
                    ╲ YES ╱                      │
                      │                          │
              ┌───────────────┐                  │
              │ RESET RTRN/RDL│                  │
              │ BIT           │                  │
              └───────────────┘                  │
                      │                          │
              ┌───────────────┐                  │
              │   SET.NEWC    │                  │
              └───────────────┘                  │
                      │                          │
              ┌───────────────┐                  │
              │ 0 → DATA (09:2)│                 │
              └───────────────┘                  │
                      │                          │
              ┌───────────────┐                  │
              │   SET.NEWC    │                  │
              └───────────────┘                  │
                      │
              ┌───────────────┐
              │   SET.NEWC    │       DELAY 2
              └───────────────┘       BAUD TIMES
                      │
              ┌───────────────┐
              │   SET.NEWC    │
              └───────────────┘
                      │
              ┌───────────────┐
              │ 1 → LL (09:3) │
              │ 1 → DATA (09:2)│
              └───────────────┘
                      │
              ┌───────────────┐
              │   SET.NEWC    │
              └───────────────┘
                      │
                ┌──────────┐    ┌──────────┐
                │   END    │    │   END    │
                └──────────┘    └──────────┘
```

```
              ╭──────────────╮
              │  PROCEDURE   │
              │   SET.NEWC   │
              ╰──────────────╯
                      │
              ┌───────────────┐
              │ 1 → NEWC (1F:0)│
              └───────────────┘
                      │
                      │◄──────────┐
                    ╱╲            │
                   ╱    ╲    NO   │
                  ╱ NEWC = 0? ╲───┘
                   ╲        ╱
                    ╲    ╱
                    ╲ YES ╱
                      │
                ┌──────────┐
                │   END    │
                └──────────┘
```
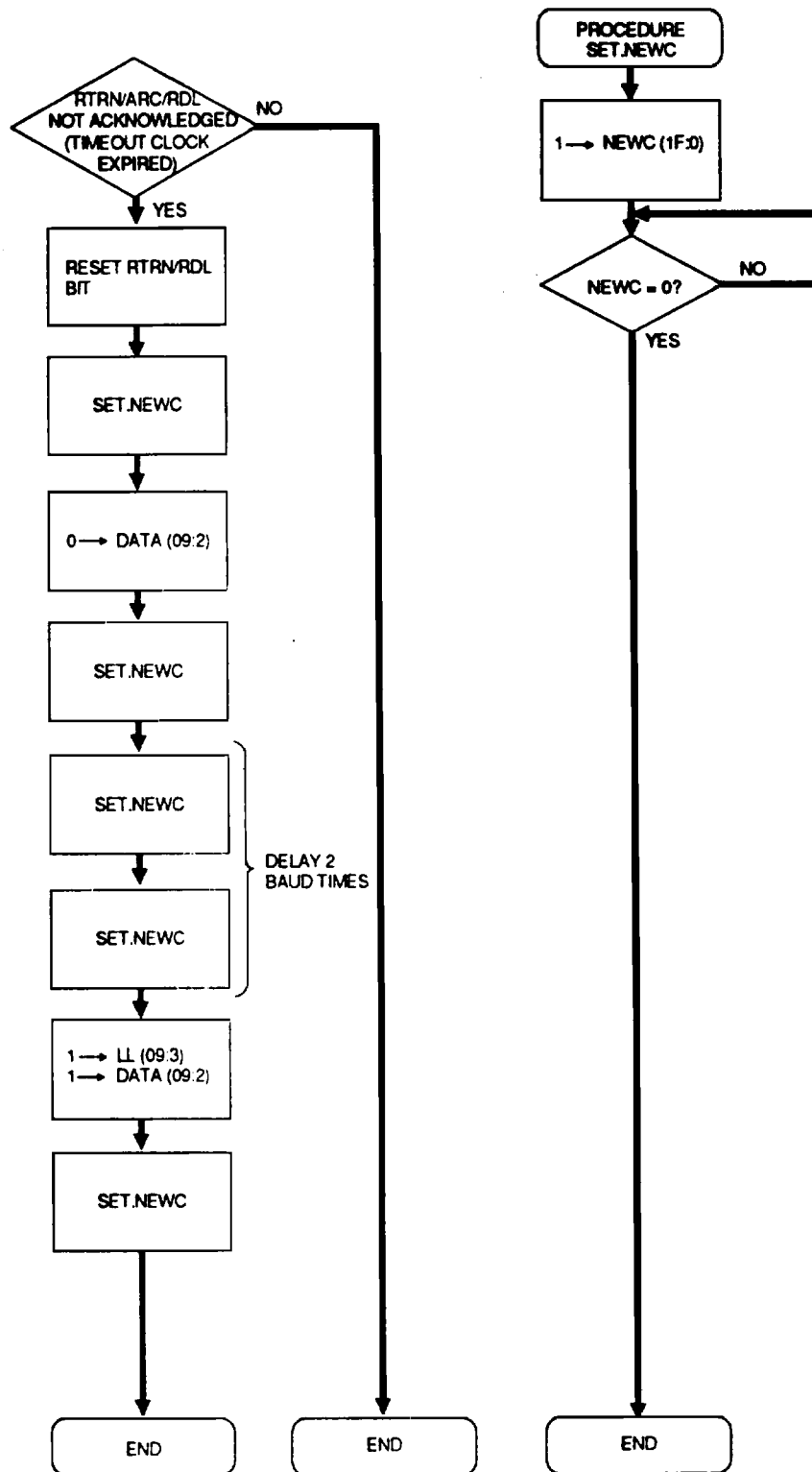
Figure 3-4. Aborting Retrain, Retrain/ARC, or RDL

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3.2 DSP RAM ACCESS

The DSP contains four sections of 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) sections, as well as data and coefficient sections. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously in either the data or coefficient section.

3.2.1 INTERFACE MEMORY ACCESS TO DSP RAM

The DSP interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The addresses stored in DSP interface memory RAM Address registers (i. e., XADD and YADD) by the host, in conjunction with the data or coefficient RAM bits (i. e., XCR and YCR) determine the DSP RAM addresses for data access.

One or two 16-bit words can be transferred between DSP RAM and DSP interface memory once each receiver sample. Two RAM access bits (XACC and YACC) in the DSP interface memory tell the DSP to access the X RAM and/or Y RAM. The DSP tests these bits each receiver sample period (1/7200 Hz).

3.2.2 HOST PROGRAMMABLE DATA

The parameters available in DSP RAM are listed in Table 3-2 along with the X RAM or Y RAM address and corresponding XCR or YCR bit value. The scaling for the host programmable data is described in Section 3.3

3.2.3 HOST DSP READ AND WRITE PROCEDURES

DSP RAM Write Procedure

The flowchart in Figure 3-5 shows the host procedure for performing a DSP RAM write to XRAM addresses. The same method may be used to write to YRAM addresses.

After the DSP has transferred the contents of the interface memory RAM data registers into DSP RAM, the DSP resets the XACC and/or the YACC bit to a 0, then sets the NEWS bit to a 1 indicate DSP RAM write completion.

If the NSIE bit is a 1, $\overline{\text{IRQ}}$ is also asserted and NSIA is set to a 1 when NEWS is set to a 1. NSIA is cleared by writing a 0 into the NEWS bit, which also causes $\overline{\text{IRQ}}$ to return high if no other interrupt requests are pending.

DSP RAM Read Procedure

The flowchart in Figure 3-6 shows the host procedure for performing a DSP RAM read from XRAM addresses. The same method may be used to read from YRAM addresses.

After the DSP has transferred the contents of RAM into the interface memory RAM data registers, the DSP resets the XACC and/or the YACC bit to a 0, then sets the NEWS bit to a 1 to indicate DSP RAM read completion.

If the NSIE bit is a 1, IRQ is also asserted and NSIA is set to a 1 when NEWS is set to a 1. NSIA is cleared by writing a 0 into the NEWS bit, which also causes IRQ to return high if no other interrupt requests are pending.
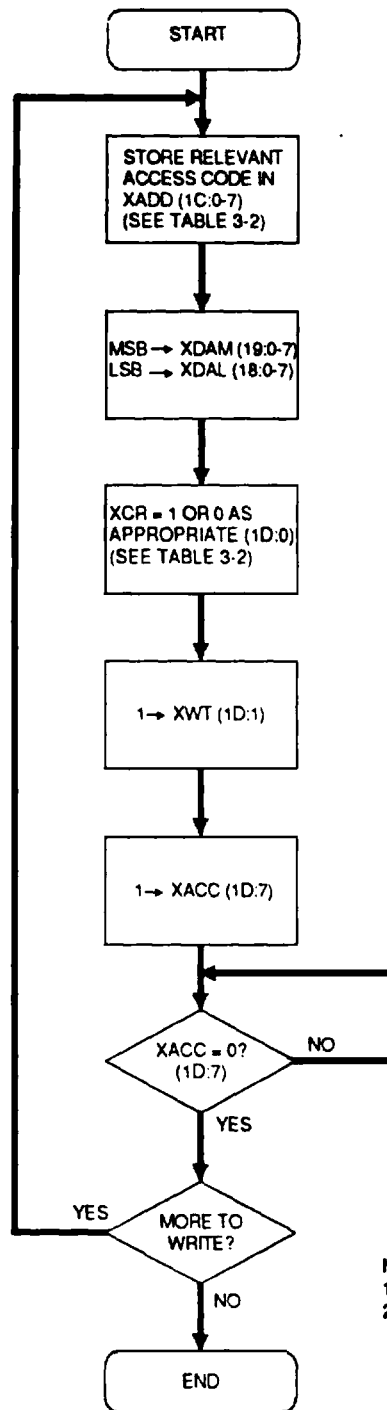
Table 3-2. DSP RAM Parameters

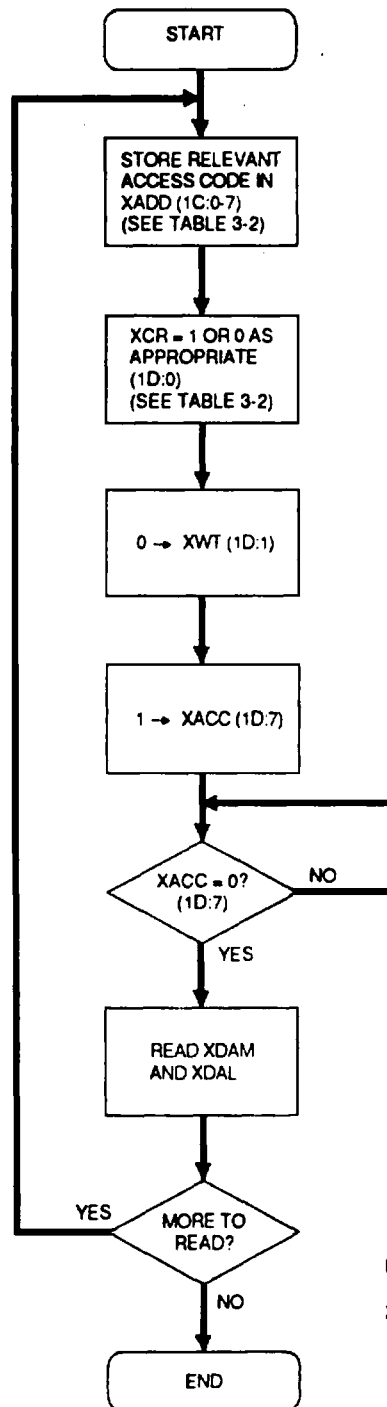| No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
1	1	0	–	1st Equalizer Tap, Real
1	1	10	–	Last Equalizer Tap, Real
2	1	–	0	1st Equalizer Tap, Imaginary
2	1	–	10	Last Equalizer Tap, Imaginary
3	0	16	–	Rotated Error, Real
4	0	–	16	Rotated Error, Imaginary
5	0	3F	–	Max AGC Gain Word
6	0	71	–	Pulse Dial Interdigit Time
7	0	7C	–	Tone Dial Interdigit Time
8	0	72	–	Pulse Dial Relay Make Time
9	0	7D	–	Pulse Dial Relay Break Time
10	0	7E	–	DTMF Duration
11	0	6D	–	Tone 1 Angle Increment Per Sample
12	0	–	6D	Tone 2 Angle Increment Per Sample
13	0	6F	–	Tone 1 Amplitude
14	0	–	6F	Tone 2 Amplitude
15	0	73	–	Max Samples Per Ring Frequency Period
16	0	74	–	Min Samples Per Ring Frequency Period
17	1	12	–	Real Part of Error
18	1	–	12	Imaginary Part of Error
19	1	–	14	Rotation Angle for Carrier Recovery
20	1	15	–	Rotated Equalizer Output, Real
21	1	–	15	Rotated Equalizer Output, Imaginary
22	1	16	–	Lower Part of Phase Error
23	1	–	16	Upper Part of Phase Error
24	1	3F	–	Upper Part of AGC Gain Word
25	1	–	3F	Lower Part of AGC Gain Word
26	1	1F	–	Average Power
27	1	2D	–	Phase Error
28	1	2F	–	Tone Power (ATBELL, BEL103 or TONEA
29	1	–	2F	Tone Detect Threshold (Call Progress Energy)
30	1	30	–	Tone Power (ATV25 or TONEB)

Table 3-2. DSP RAM Parameters (Cont'd)

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
31	1	31	–	Tone Power (TONEC)
32	1	36	–	Tone Detect Threshold (ATBELL, BEL103, or TONEA)
33	1	37	–	Tone Detect Threshold (ATV25 or TONEB)
34	1	38	–	Tone Detect Threshold (TONEC)
35	1	3B	–	Zero Crossing Counter
36	1	52	–	Eye Quality Monitor (EQM)
37	1	–	31	Filter 1 Coefficient $\alpha0$
38	1	–	32	Filter 1 Coefficient $\alpha1$
39	1	–	33	Filter 1 Coefficient $\alpha2$
40	1	–	34	Filter 1 Coefficient $\beta1$
41	1	–	35	Filter 1 Coefficient $\beta2$
42	1	–	37	Filter 2 Coefficient $\alpha0$
43	1	–	38	Filter 2 Coefficient $\alpha1$
44	1	–	39	Filter 2 Coefficient $\alpha2$
45	1	–	3A	Filter 2 Coefficient $\beta1$
46	1	–	3B	Filter 2 Coefficient $\beta2$
47	1	–	76	Filter 3 Coefficient $\alpha0$
48	1	–	77	Filter 3 Coefficient $\alpha1$
49	1	–	78	Filter 3 Coefficient $\alpha2$
50	1	–	79	Filter 3 Coefficient $\beta1$
51	1	–	7A	Filter 3 Coefficient $\beta2$
52	1	–	45	Filter 4 Coefficient $\alpha0$
53	1	–	46	Filter 4 Coefficient $\alpha1$
54	1	–	47	Filter 4 Coefficient $\alpha2$
55	1	–	48	Filter 4 Coefficient $\beta1$
56	1	–	49	Filter 4 Coefficient $\beta2$
57	1	1C	–	Turn-on Threshold (PSK)
58	1	32	–	Turn-off Threshold (PSK)
59	1	–	21	RLSD Turn-off Time (PSK)
60	0	–	1C	Turn-on Threshold (FSK)
61	0	–	1D	Turn-off Threshold (FSK)
62	0	70	–	Transmit Level Output Attenuation

* XCR if an XRAM address is listed; YCR if a YRAM address is listed.

START

STORE RELEVANT
ACCESS CODE IN
XADD (1C:0-7)
(SEE TABLE 3-2)

MSB → XDAM (19:0-7)
LSB → XDAL (18:0-7)

XCR = 1 OR 0 AS
APPROPRIATE (1D:0)
(SEE TABLE 3-2)

1 → XWT (1D:1)

1 → XACC (1D:7)

XACC = 0?
(1D:7)   NO

YES

MORE TO
WRITE?   YES

NO

END

NOTE:
1) ALSO APPLICABLE FOR YRAM ACCESS.
2) XCR, XWT, AND XACC BITS CAN ALL BE
   CONFIGURED DURING THE SAME
   REGISTER ACCESS (1D).

Figure 3-5. XRAM Write Routine

```
                    ┌─────────────┐
                    │    START    │
                    └──────┬──────┘
                           │
                           ▼
                  ┌──────────────────┐
                  │ STORE RELEVANT   │
                  │ ACCESS CODE IN   │
                  │ XADD (1C:0-7)    │
                  │ (SEE TABLE 3-2)  │
                  └────────┬─────────┘
                           │
                           ▼
                  ┌──────────────────┐
                  │ XCR = 1 OR 0 AS  │
                  │ APPROPRIATE      │
                  │ (1D:0)           │
                  │ (SEE TABLE 3-2)  │
                  └────────┬─────────┘
                           │
                           ▼
                  ┌──────────────────┐
                  │  0 → XWT (1D:1)  │
                  └────────┬─────────┘
                           │
                           ▼
                  ┌──────────────────┐
                  │  1 → XACC (1D:7) │
                  └────────┬─────────┘
                           │
                           ▼
                      ╱XACC = 0?╲    NO
                      ╲ (1D:7)  ╱──────┐
                          │YES
                          ▼
                  ┌──────────────────┐
                  │  READ XDAM       │
                  │  AND XDAL        │
                  └────────┬─────────┘
                           │
                  YES      ▼
              ┌────────╱ MORE TO ╲
              │        ╲  READ?  ╱
              │            │NO
              │            ▼
              │      ┌───────────┐
              │      │    END    │
              │      └───────────┘
```

NOTE:
1) ALSO APPLICABLE FOR YRAM ACCESS.
2) XCR, XWT, AND XACC BITS CAN ALL BE
   CONFIGURED DURING THE SAME
   REGISTER ACCESS (1D).

Figure 3-6. XRAM Read Routine

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3.3 DIAGNOSTIC DATA SCALING

The scaling of the host programmable parameters listed in
Table 3-2 is described in this section.

No. 1 - Equalizer Tap Coefficients, Real   XCR: 1   XRAM Addr: 0 - 10

The adaptive equalizer is a transversal filter (Figure 3-7). The filter is tuned by varying the weighting coefficients, C_0 through C_N. The modem has 17 taps. Since the baseband signal is complex it requires both X and Y coefficients for each tap. The delay between taps is 1/2 baud time. The adaptive process attempts to adjust all coefficients to minimize the mean squared error.
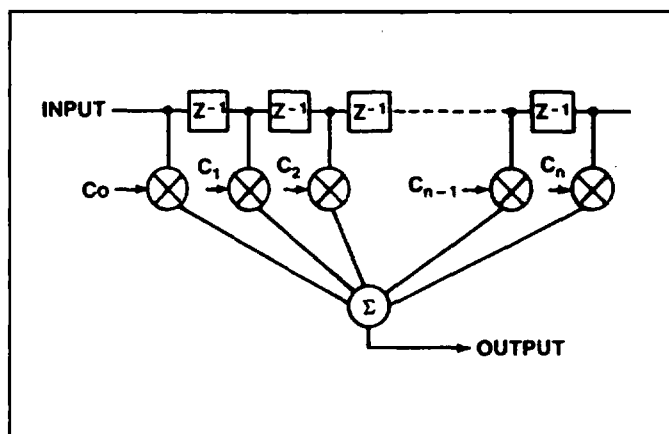
Figure 3-7. Equalizer Structure

No. 2 - Equalizer Tap Coefficients, Imaginary   YCR: 1   YRAM Addr: 0 - 10

These values represent the imaginary component of the equalizer tap coefficients. (See above.)

No. 3 - Rotated Error, Real   XCR: 0   XRAM Addr: 16

The Rotated Error vector is the angle and magnitude difference between an actual received signal point (P2) and the nearest ideal point (P1) in the baseband signal plane (Figure 3-8) after the signal has been corrected for rotational error. The real and imaginary components are calculated once per baud time. See Real Part of Error (No. 17) and Imaginary Part of Error (No. 19).

$$P_1 = x_1 + iy_1$$
$$P_2 = x_2 + iy_2$$
$$P_2 - P_1 = (x_2 - x_1) + i(y_2 - y_1)$$
$$= \text{REAL ERROR} + \text{IMAGINARY ERROR}$$
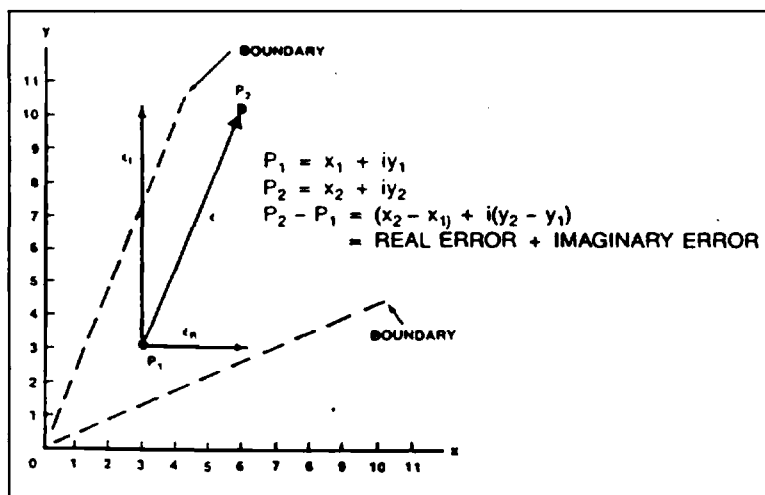
Figure 3-8. Rotated Error

No. 4 - Rotated Error, Imaginary	YCR:	0	YRAM Addr:	16

These values represent the imaginary component of the Rotated Error vector. (See No. 3.)

No. 5 - Max AGC Gain Word	XCR:	0	XRAM Addr:	3F

Default: $2500 (31.95 dB)
This value represents the maximum AGC gain, and can be varied by the host.

Formula:

$$\text{Max AGC Gain Word} = (46.4 - \text{Max AGC Gain (dB)}) \times 32768/50$$

Convert value to hex to store in RAM.

No. 6 - Pulse Dial Interdigit Time	XCR:	0	XRAM Addr:	71

Default: $1518 (750 ms)
This value represents the amount of delay in samples between digits dialed when in pulse dial mode (DTMF = 0).

Formula:

$$\text{Interdigit time (samples)} = \text{Interdigit time (sec)} \times 7200 \text{ (samples/sec)}$$

Convert sample value to hex to store in RAM.

No. 7 - Tone Dial Interdigit Time	XCR:	0	XRAM Addr:	7C

Default: $01F8 (70 ms)
This value represents the amount of delay in samples between digits dialed when in tone dial mode (DTMF = 1).
Formula:

$$\text{Interdigit Time (samples)} = \text{Interdigit Time (sec)} \times 7200 \text{ (samples/sec)}$$

Convert sample value to hex to store in RAM.

No. 8 - Pulse Dial Relay Make Time	XCR:	0	XRAM Addr:	72

Default: $0120 (40 ms)
This value represents the time (in number of samples) that the $\overline{\text{OHRELAY}}$ will close for each digit dialed.

Formula:

$$\text{Pulse Make Time (samples)} = \text{Pulse Make Time (sec)} \times 7200 \text{ (samples/sec)}$$

Convert sample value to hex to store in RAM.

No. 9 - Pulse Dial Relay Break Time	XCR:	0	XRAM Addr:	7D

Default: $01B0 (60 ms)
This value represents the time (in number of samples) that the $\overline{\text{OHRELAY}}$ will open for each digit dialed.

Formula:

$$\text{Pulse Break Time (samples)} = \text{Pulse Break Time (sec)} \times 7200 \text{ (samples/sec)}$$

Convert sample value to hex to store in RAM.

No. 10 - DTMF Duration	XCR:	0	XRAM Addr:	7E

Default: $01F8 (70 ms)
This value represents the time duration of each DTMF digit dialed.

Formula:

$$\text{DTMF duration (samples)} = \text{DTMF duration (sec)} \times 7200 \text{ (samples/sec)}$$

Convert value to hex to store in RAM.

No. 11- Tone 1 Angle Increment per Sample	XCR:	0	XRAM Addr:	6D
No. 12 - Tone 2 Angle Increment per Sample	YCR:	0	YRAM Addr:	6D

Default: $00

When the host enters Tone Generation/Detection mode (CONF = 80), the transmitter immediately begins sending the dual tone frequencies specified by addresses XRAM 6D and YRAM 6D with amplitudes specified by XRAM 6F and YRAM 6F, respectively. The tones will remain on as long as Tone Generation/Detection mode is specified and the amplitudes are greater than zero. If the host reconfigures to Tone Generation/Detection mode after dialing a digit in Dial/Call Progress mode, the modem will send the dual tone of the last digit dialed until the values in XRAM 6F and YRAM 6F are set to 0.

Frequencies from 0 Hz to 1675 Hz can only be sent when the ORG bit is set, and frequencies from 1925 Hz to 2875 Hz can only be sent when the ORG bit is cleared. 1800 Hz frequency can be sent by setting the GTE bit with GTS=0 and ORG = 0.

To calculate the frequency value to store in RAM, follow the steps below:

1. Find Phase Angle Increment in degrees/sample:

   Angle (degrees/sample) = Frequency (Hz) x (360 degrees/cycle)/7200 (samples/second)

2. Scale result as follows:

   Angle Increment (increment/sample) = Angle (degrees/sample) x (32768/180 degrees)

3. Round off Angle Increment.

4. Convert to hex and store in RAM.

Example: For 1300 Hz,

1. Angle (degrees/sample) = 1300 Hz x 360 (degrees/cycle)/7200 samples/sec = 65 (degrees/sample).

2. Angle Increment (increment/sample) = 65 (degrees/sample) x (32768/180 degrees) = 11832.9 increment/sample.

3. Value to store in RAM = $2E39 (11833).

Note: The ORG bit must be set to generate 1300 Hz tone.

No. 13 - Tone 1 Amplitude	XCR:	0	XRAM Addr:	6F
No. 14 - Tone 2 Amplitude	YCR:	0	YRAM Addr:	6F

Default: $00

These values determine the amplitude of the two tones that are immediately sent when the host enters into Tone Generation/Tone Detection mode. The amplitude of each tone can range from 9.1 dBm down to approximately –50 dBm. The relationship between the output in dBm and the RAM amplitude value for a single tone frequency is shown in Figure 3-9 for a TLVL (13:4-7) value of 0. Changing TLVL further adjusts the output tone level. Setting one of the two amplitudes to zero selects single tone frequency.

The DTMF levels and the transmit level of the 1300 Hz calling tone is 6 dB under the data transmit level. The modem loads the value $1800 into Tone 1 Amplitude (XRAM address $6F, XCR = 0) to generate a calling tone that is 6 dB less than TLVL. If the host wishes to generate a calling tone that is at the same level as the data transmit level, the host must write a value of $3000 into this location. The procedure is:

1. Wait until TDBE signals that the previous digit is dialed.

2. Write to XRAM address $7C (XCR = 0) and XRAM address $7E (XCR=0) to control the tone Off and On time, respectively.

3. Write $3000 into XRAM $6F, XCR = 0.

4. Write the digit to be dialed into TBUFFER.

5. Poll XRAM address $6F until the $3000 value is changed to $1800 by the modem.

6. Write $3000 again into XRAM $6F, XCR = 0.

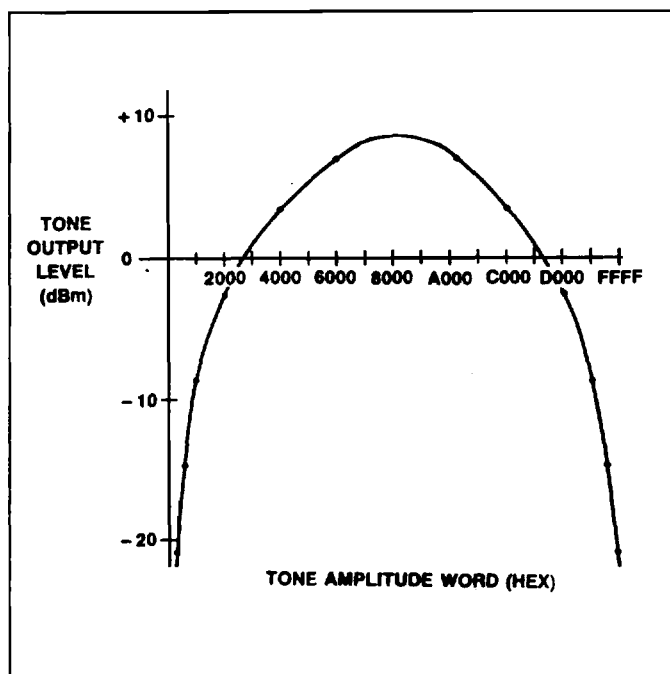Repeat steps 1 - 6 each time a digit is loaded into TBUFFER.

Figure 3-9. Tone Output Level versus Tone Amplitude

No. 15 - Maximum Samples per Ring Frequency Period	XCR:	0	XRAM Addr:	73

Default: $0202 (71.4 ms)

This value determines the maximum period of the signal on RD that will be indicated on RI and $\overline{\text{RI}}$. The default value of 71.4 ms corresponds to a minimum ring frequency of 14 Hz. This allows proper detection of frequencies as low as 15 Hz.

Formula:

Maximum period samples = 7200 (samples/sec)/minimum ring frequency (Hz)

Convert maximum samples to hex to store in RAM.

No. 16 - Minimum Samples per Ring Frequency Period	XCR:	0	XRAM Addr:	74

Default: $0064 (13.9 ms)

This value determines the minimum period of the signal on RD that will be indicated on RI and $\overline{\text{RI}}$. The default value of 13.9 ms corresponds to a maximum ring frequency of 72 Hz. This allows proper detection of frequencies as high as 68 Hz.

Formula:

Minimum period samples = 7200 (samples/sec)/maximum ring frequency (Hz)

Convert minimum samples to hex to store in RAM.

No. 17 - Real part of Error	XCR:	0	XRAM Addr:	12
No. 18 - Imaginary Part of Error	YCR:	0	YRAM Addr:	12

The Error Vector is the angle and magnitude difference between the received signal point and the nearest ideal point before the signal has been corrected for rotational error (see Rotated Error, No. 3 and No. 4). Rotational error is caused by phase and frequency differences between the transmitter and receiver carrier signals.

No. 19 - Rotation Angle for Carrier Recovery   YCR: 1   YRAM Addr: 14

The Rotation Angle represents correction for both absolute phase differences and continuously changing phase differences.

Formula:

         Rotation Angle (degrees) = [(Rotation Angle Word/$FFFF)$_{DEC}$ x 360

Where 0° ≤ Rotated Angle ≤ 360°

No. 20 - Real Rotated Equalizer Output   XCR: 1   XRAM Addr: 15
No. 21 - Imaginary Rotated Equalizer Output   YCR: 1   YRAM Addr: 15

These values represent the received points after decoding by the decision logic. The points are compared to the ideal points stored in ROM. Figures 3-10 through 3-12 show the locations of the ideal baseband points. The machine unit values represent signal scaling for all baseband signals.

No. 22 - Lower Part of Phase Error   XCR: 1   XRAM Addr: 16
No. 23 - Upper Part of Phase Error   YCR: 1   YRAM Addr: 16

This Phase Error value is the intermediate output of the second order carrier recovery loop.

No. 24 - Upper Part of AGC Gain Word   XCR: 1   XRAM Addr: 3F
No. 25 - Lower Part of AGC Gain Word   YCR: 1   YRAM Addr: 3F

This information represents the gain of the AGC amplifier. The upper part of the AGC gain uses the same formula as the Max AGC Gain Word (No. 5). The lower part of the AGC gain can be used for better precision.

Formula:

         AGC Gain (dB) = 46.4 - (Upper part of AGC Gain word)$_{DEC}$ x 50/32768

No. 26 - Average Power   XCR: 1   XRAM Addr: 1F

This value represents the average received signal power. It can be scaled from engineering units to units of dBm. Use AGC Gain Word (No. 24 and No. 25) to calculate the pre-AGC gain.

Formula:

         Post-AGC Average Power (dBm) = 10 LOG [(Power Word)/(2 x $889)]$_{DEC}$
         Pre-AGC Gain Average Power (dBm) = Post AGC Gain Power - AGC Gain

XRAM Address 1C is also used to measure call progress energy detect power in the call detection mode for the Tone A bit.

No. 27 Phase Error   XCR: 1   XRAM Addr: 2D

This Phase Error is the input to the second order carrier recovery loop.

No. 26 - Tone Power (TONEA/CALL PROGRESS MODE)   XCR: 1   XRAM Addr: 1F
No. 28 - Tone Power (ATBELL, BEL103, or TONEA/TONE MODE)   XCR: 1   XRAM Addr: 2F
No. 30 - Tone Power (ATV25, TONEB)   XCR: 1   XRAM Addr: 30
No. 31 - Tone Power (TONEC)   XCR: 1   XRAM Addr: 31

These values represent Post-AGC tone power measurement. Since the tone filters are available only in certain modes, these RAM locations are shared for tone power. Table 3-3 lists the tone power locations for each mode.

Formula:

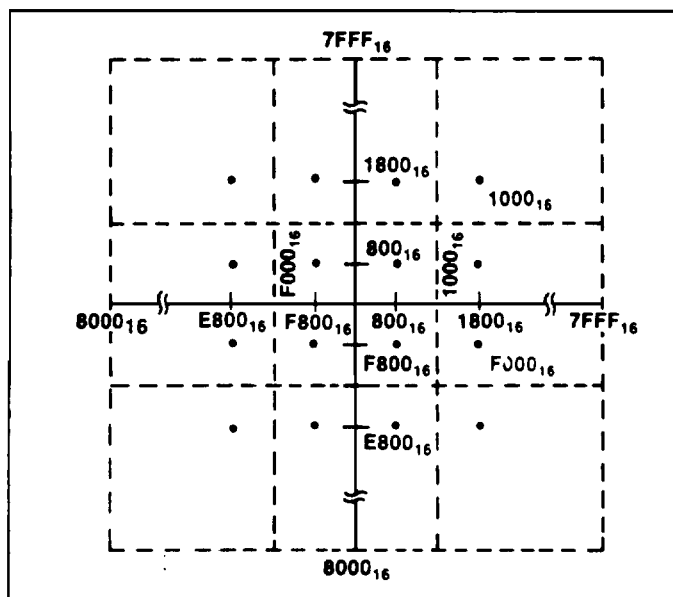   Post-AGC Tone Power (dBm) = 10 LOG [(Tone Power Word)/(2 x $889)]$_{DEC}$
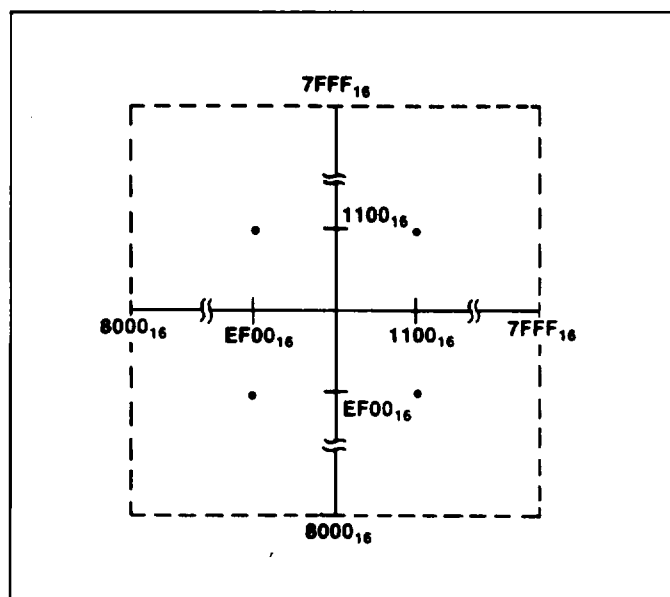
Figure 3-10. Ideal Points-V.22 bis 2400 bps

Figure 3-11. Ideal Points-V.22 A/B, Bell 212A 1200 bps

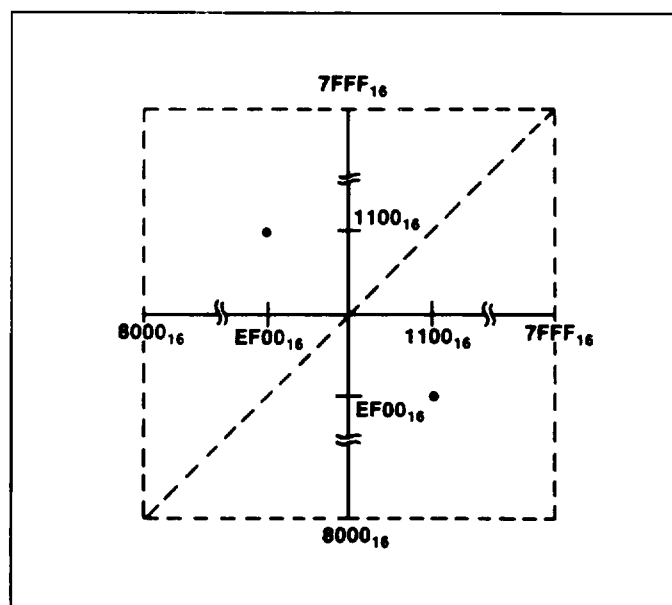Figure 3-12. Ideal Points-V.22 A/B 600 bps

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No. 29 - Tone Detect Threshold (Call Progress Energy)	YCR:	1	YRAM Addr:	2F
No. 32 - Tone Detect Threshold (ATBELL, BEL103, or TONEA)	XCR:	1	XRAM Addr:	36
No. 33 - Tone Detect Threshold (ATV25 or TONEB)	XCR:	1	XRAM Addr:	37
No. 34 - Tone Detect Threshold (TONEC)	XCR:	1	XRAM Addr:	38

Some RAM locations are shared for the tone detect threshold in different modes. Table 3-3 lists the tone detect threshold locations for each mode. The threshold word is defined as a function of the change in threshold level.

Formula:

New Threshold Word = (Old Threshold Word)$_{DEC}$ EXP (change in dB/10)

Convert value to hex to store in RAM

The host has only limited control of the tone detect threshold with these access codes. To vary the threshold to a greater degree, the host must write to the Max AGC Gain Word (No. 5).

Table 3-3. Digital Filter Access Codes

Mode	Tone Detect Threshold Address	Tone Power Address	Filter Status Bit	Filter Coefficient	Default Tone Detect (Hz)
Dial/Call Progress	2F	1F	TONEA	1, 2	335-645
	36	2F	ATBELL (ORG=1)	3	2225
	36	2F	BEL103 (ORG=0)	3	1270
	37	30	ATV25	4	2100
Tone Generation/ Detection	36	2F	TONEA	1	1300
	37	30	TONEB	2	390
	38	31	TONEC	3	980 (ORG=0),1650 (ORG=1)
Handshake	36	2F	ATBELL (ORG=1)	3	2225
	36	2F	BEL103 (ORG=0)	3	1270
	37	30	ATV25	4	2100

Note: The host should set/clear the ORG bit before entering Tone Generation/Detection mode or Dial/Call Progress mode. When re-configuring from Dial/Call Progress mode to Tone Generation/ Detection mode, the host must first configure the modem for V.22 bis mode (CONF = 84) to initialize the tone detect filters.

No. 35 - Zero Crossing Detector	XCR:	1	XRAM Addr:	3B

The zero crossing detector is always available. The detector can measure tone frequencies between 100 Hz and 3000 Hz, and increments for both positive and negative zero crossings. To use the detector, the host writes $00 to the detector at location 38, delays for some amount of time, and then reads the value at location 38. The value read is ±1 crossing of the actual value. Note that the zero crossing detector will increment any time the received signal crosses zero.

No 36 - Eye Quality Monitor Output	XCR:	1	XRAM Addr:	52

The error vector formed by the decision logic can be used to indicate relative signal quality. As signal quality deteriorates, the average error vector increases in magnitude. By calculating the magnitude of the error vector and filtering the results, a number inversely proportional to signal quality is derived. This number is called the Eye Quality Monitor (EQM). Because of the filter time constant, EQM should be allowed to stabilize for approximately 700 baud times following RLSD going active.

The EQM value is the filtered squared magnitude of the error vector and represents the average signal power contained in the error component. The power is directly proportional to the probability of errors occurring in the received data and can be used to implement a discrete Data Signal Quality Detector circuit (circuit 110 of CCITT V.24 or circuit CG of RS-232-C) by comparing the EQM value against experimentally determined criteria (bit error rate curves). (See Figure 3-13.)

 illustrates the relationship of the EQM number to an eye pattern created by a four-point signal structure (e.g., Bell 212A/1200 bps) in the presence of high level white noise. The EQM value is proportional to the square of the radius of the disk around any ideal point. The radius increases when signal-to-noise ratio (SNR) decreases. As the radius approaches the ideal points' boundary values, the bit error rate (BER) increases. Curves of BER as a function of the SNR are used to establish a criteria for determining the acceptability of EQM values. Therefore, from an EQM value, the host processor can determine an approximate BER value. If the BER is found to be unacceptable, the host may cause the modem to fall back to a lower speed to improve BER.

It should be noted that the meaning of EQM varies with the type of line disturbances present on the line and with the various configurations. A given magnitude of EQM in V.22 bis/2400 does not represent the same BER as in V.22/1200. The former configuration has 16 points that are more closely spaced than the four signal points in the latter, resulting in a greater probability of error for a given level of noise or jitter. Also, the type of line disturbance has a significant bearing on the EQM value. For example, white noise produces an evenly distributed smearing of the eye pattern with about equal magnitude and phase error while phase jitter produces phase error with little error in magnitude.

Since EQM is dependent upon the signal structure of the modulation being used and the type of line disturbance, EQM must be determined empirically in each application.
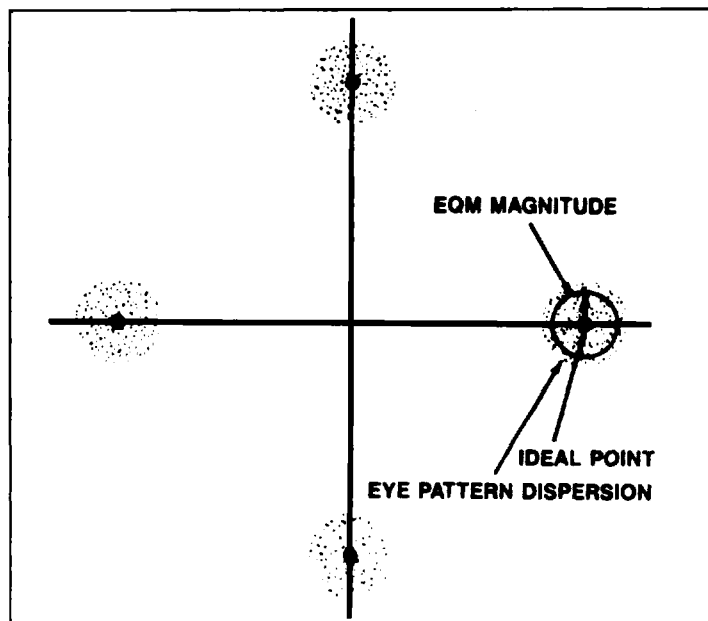
Figure 3-13. Relationship of EQM to Eye Pattern

Nos. 37 - 56 Digital Filter Coefficients   **YCR: 1   YRAM Addr: (See Table 3-2)**

The digital filters in all modes are fully programmable single biquad IIR filters, except for the Call Progress Monitor - Tone A in Dial/Call Progress mode which is a dual biquad IIR filter. All of the biquad filters follow the following transfer function:

$$H(z) = 2 (\alpha_0 + \alpha_1 Z^{-1} + \alpha_2 Z^{-2})/(1 - \beta_1 Z^{-1} - 2\beta_2 Z^{-2})$$

Table 3-3 shows which filter coefficients correspond to the tone detect status bits in each mode. The modem will load default values each time the host changes modes. Table 3-4 shows calculated coefficient values for default tone detect filters. These values are scaled so that the coefficients of the transfer function are divided by the maximum register value. For example, α_0 for 2225 Hz is $(0666/7FFF)_{DEC} = 0.04999$. Coefficient values greater than 7FFF represent twos complement negative numbers.

Table 3-4. Calculated Tone Detect Values

Frequency Detected (Hz)	Coefficient Values				
	α_0	α_1	α_2	β_1	β_2
2225	0666	02A6	0418	D28A	C289
2100	0666	03B6	0418	DF89	C289
1650	044E	FD17	02C1	105F	C28A
1300	05D1	FA77	03B9	3502	C289
1270	05D1	FA77	0389	37F8	C289
980	0572	FC52	037C	524B	C28A
390	06EC	F4F3	046E	763D	C28A

No. 57 - Turn-on Threshold (PSK)	XCR:	1	XRAM Addr:	1C
No. 60 - Turn-on Threshold (FSK)	YCR:	0	YRAM Addr:	1C

The Turn-on Threshold Word determines the receive level at which carrier is detected (RLSD turns on). The Threshold Word is a function of the change in threshold level. The host has only limited control of the Turn-on Threshold through this parameter. To vary the threshold to a greater extent, write to the Max AGC Gain Word (No. 5).

Formula:

$$\text{New Threshold Word} = \text{(Old Threshold Word)}_{DEC} \text{ EXP (Change in dB/10)}$$

Convert value to hex to store in RAM.

No. 58 - Turn-off Threshold (PSK)	XCR:	1	XRAM Addr:	32
No. 61 - Turn-off Threshold (FSK)	YCR:	0	YRAM Addr:	1D

The Turn-off Threshold Word determines the receive level at which carrier is not detected (RLSD turns off). The Threshold Word is a function of the change in threshold level. The host has only limited control of the Turn-off Threshold through this parameter. To vary the threshold to a greater extent, write to the Max AGC Gain Word (No. 5).

Formula:

$$\text{New Threshold Word} = \text{(Old Threshold Word)}_{DEC} \text{ EXP (Change in dB/10)}$$

Convert value to hex to store in RAM.

No. 59 - RLSD Turn-off Time (PSK)	YCR:	1	YRAM Addr:	21

Default: $0002

The RLSD Turn-off Time is the time (in number of samples) between when the received carrier falls below the Turn-off threshold and when RLSD turns off.

$$\text{RLSD Turn-off Time (Samples)} = \text{RLSD Turn-off Time (sec)} \times 7200 \text{ (Samples/sec)}$$

Convert value to hex to store in RAM.

No. 62 - Transmit Level Output Attenuation	XCR:	0	XRAM Addr:	70

Default: $7200

When TLVL (13:4-7) is set to an odd number, the value in this location determines the change in attenuation from the next highest even TLVL value.

Formula:

$$\text{New Level Attenuation Word} = \text{(Old Level Attenuation Word)}_{DEC} \text{ EXP (Change in dB/10)}$$

3.4 SOFTWARE INTERFACE CONSIDERATIONS

3.4.1 POWER-ON/RESET DSP TEST MODE

After Power-on or Reset, the modem enters into a test mode and calculates checksum on ROM. The result of the checksum verification is written to interface memory bytes 15 and 14. The valid checksum is a constant $412B.

At the same time, ASCII values corresponding to the "device part number" are written to interface memory byte 13 and 12, and ASCII values for the "code revision letter" are written to interface memory bytes 11 and 10. For example, for the C5312-16 "C" code device, the number "12" is the part number and the letter "C" is the code revision letter. The values written into interface memory would be:

Register	Value	Contents
15	$41	Checksum upper word
14	$2B	Checksum lower word
13	$31	ASCII value for "1"
12	$32	ASCII value for "2"
11	$20	ASCII value for " "
10	$43	ASCII value for "C"

If the host reads the revision letter after Power-On-Reset, then the host should select analog loopback mode immediately after the POR sequence and read the RBUFFER in order to clear the character loaded into the TBUFFER.

After the DSP writes to byte 10, the TDBE bit is set. This indicates to the host that the self-test information can be read. The DSP will wait 20 ms or until the host reads or writes interface memory byte 10. After this the DSP executes the initialization sequence.

3.4.2 INTERRUPT REQUEST HANDLING

DSP interface memory registers 00, 10, 1E, and 1F have unique hardware connections to the interrupt logic. Register 00 is the Receive Buffer (RBUFFER) and register 10 is the Transmit Buffer (TBUFFER). Registers 1E and 1F hold interrupt flag, interrupt enable, and interrupt active bits.

When a condition occurs that satisfies an interrupt criteria, the corresponding interrupt flag bit is set. This interrupt flag can be reported to the host either by the host polling the interrupt flag bits (i.e., not using IRQ) or by being interrupted by IRQ. When an interrupt enable bit and the corresponding interrupt flag are both set to a 1, IRQ is asserted and the corresponding interrupt active bit set to a 1.

The interrupt flag setting conditions are status changed detected, configuration changed acknowledged, receive buffer full and transmit buffer empty. Table 3-5 identifies the interrupt conditions and bits, and describes the interrupt clearing procedures.

Table 3-5. Interrupt Request Bits

| Interrupt Active Bit	Interrupt Enable Bit	Interrupt Flag Bit	Interrupt Condition Description	Interrupt Clear Procedure
NSIA	NSIE	NEWS	New status detected (NEWS transitioned from a 0 to 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A, 0B, 0E, or 0F	Host writes a 0 into NEWS (Clears NSIA to a 0)
NCIA	NCIE	NEWC	New configuration acknowledged by DSP (NEWC transitioned from a 1 to a 0)	Host writes a 0 into NCIE (Clears NCIA to a 0)
TDBIA	TDBIE	TDBE	Transmitter Data Buffer is empty and can be written (TDBE transitioned from a 0 to a 1)	Host writes to register 10 (TBUFFER) (Clears TDBE and TDBIA to 0) or host resets TDBIE (Clears TDBIA to a 0)
RDBIA	RDBIE	RDBF	Receiver Data Buffer is full and can be read (RDBF transitioned from a 0 to a 1)	Host reads from register 00 (RBUFFER) (Clears RDBF and RDBIA to 0)

3.4.3 DIAL PROCEDURE

The host dial procedure is the same as outputting data to be transmitted using TBUFFER (Figure 3-14). The modem timing accounts for the DTMF tone duration and amplitude, pulse make/break ratio, and interdigit delay. These dialing parameters are host programmable in DSP RAM.

The level of the high DTMF tone is 2 dB greater than the level of the low DTMF tone.

The dialer default parameters are given in Table 3-6.

Table 3-6. Dial Default Parameters

Parameter	Default Value
DTMF Tone Duration	70 ms
DTMF Interdigit Delay	70 ms
DTMF Total Output Power Level	0 dBm
DTMF Low Band Power Level	– 4 dBm
DTMF High Band Power Level	– 2 dBm
Pulse Relay Make Time	40 ms
Pulse Relay Break Time	60 ms
Pulse Interdigit Delay	750 ms
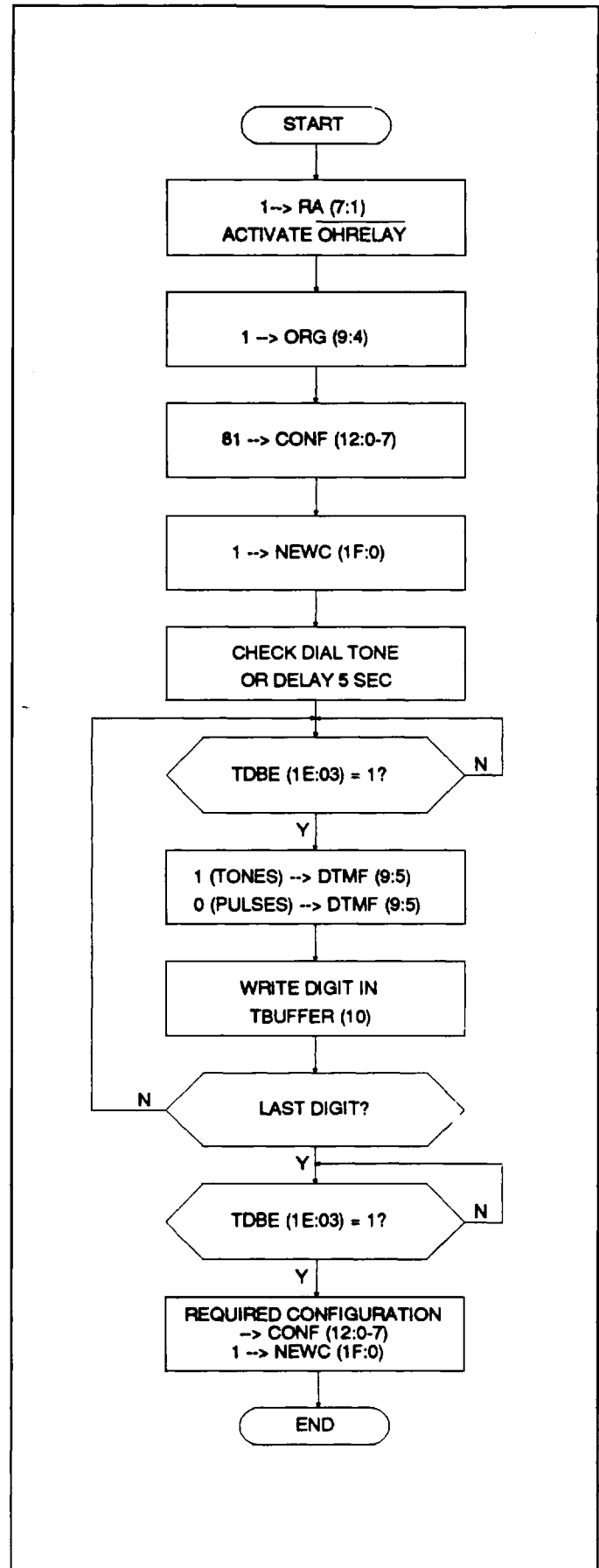
Figure 3-14. Dial Sequence

4. HDLC FEATURES

The HDLC (High Level Data Link Control) protocol is a standard procedure used for data communications. SDLC (Synchronous Data Link Control) is a bit-oriented protocol which is a subset of HDLC. The same format is used in both protocols although all SDLC fields must be eight-bit octets. The modem uses the SDLC protocol but it is referred to as HDLC to avoid confusion.

4.1. HDLC FRAMES

Data and control information on a HDLC link are transmitted via frames. These frames organize the information into a format specified by an ISO standard that enables the transmitting and receiving station to synchronize with each other. This format is shown in Figure 4-1. Flags and the frame check sequence are distinguished from the other fields by status bits in the modem interface memory.

FLAG	ADDR	CONTROL	INFORMATION	16-BIT FCS	FLAG

FRAME STARTS   FRAME ENDS

Figure 4-1. HDLC Frame

FLAGS

All frames start and end with a flag sequence. The beginning flag and the ending flag are defined by the bit pattern 01111110 (7E). The ending flag for one frame can also serve as the beginning flag for the following frame. If separate ending and beginning flags are used, the final zero in the ending flag of one frame may also serve as the first zero of the beginning flag in the following frame. This process is known as "zero-sharing". The zero-sharing bit pattern is 011111101111110.

ADDRESS FIELD

The address field informs the receiver where the information is to go (if the primary station is transmitting) or where the message originated (if a secondary station is transmitting). This field is eight bits in length for the "basic" format.

For the "extended" format, the length is N number of octets, each octet having the first bit a binary zero with the exception of the last octet that begins with a binary one.

CONTROL FIELD

The control field defines the function of the frame. It may contain a command or response. The control field might also contain send or/and receive sequence numbers. This field can be in one of the following formats:

1. Information Transfer Format

2. Supervisory Format

3. Unnumbered Format

This field is normally eight bits in length. Certain protocols allow for an extended control field of 16 bits in length.

INFORMATION FIELD

The modem does not distinguish between the address field, the control field, or the information field. The information field does not have a set length; however, this field follows the SDLC protocol in being in the format of eight bit bytes.

ZERO INSERTION

Since flags mark the beginning and ending of a frame, some method must be implemented to inhibit or alter the transmission of data that appear as flags. The method used is called "zero insertion". HDLC procedures require that a zero be transmitted following any succession of five continuous ones. This includes all data in the address, control, information and Frame Check Sequence fields. Use of zero insertion denies any pattern of 01111110 to ever be transmitted between beginning and ending flags.

The modem transmitter always performs zero insertion when in HDLC mode.

ZERO DELETION

When transmitting flags, zero insertion is disabled. During reception of data, after testing for flag recognition, the receiver removes a zero that immediately follows five continuous ones. This is termed "zero deletion". A one that follows five continuous ones signifies either a frame abort (i.e., at least seven ones with no zero insertion) or a flag (i.e., 01111110). The sixth one is, therefore, not removed.

The modem receiver always performs zero deletion when in HDLC mode.

FRAME CHECK SEQUENCE

The purpose of the Frame Check Sequence (FCS) is to give a shorthand representation of the entire transmitted information field and to compare it to the identically generated shorthand representation of the received sequence. If any difference occurs, the received frame was in error and should be re-transmitted.

The FCS computation is done on all fields within the frame but does not include the flags. Cyclic Redundancy Check (CRC) is the method used. The polynomial is specified in SDLC and X.25 as follows:

$$x^{16} + x^{12} + x^5 + 1$$

The polynomial is implemented as shown in Figure 4-2.

The Frame Check Sequence is sent as two bytes of data immediately preceding the ending flag of the frame. The FCS register is first preset to all binary ones. The register is then modified by shifting in the data (no flags) contained in the address, control, and information fields. Following the last bit of data, the ones complement of the FCS

register is transmitted as the 16-bit FCS. The FCS is transmitted with the highest order bit (x^{15}) first.

FRAME ABORTION, FRAME IDLE, AND TIME FILL

Frame abortion prematurely finishes transmission of a frame. This occurs by sending at least seven consecutive ones with no zero insertion. This abort pattern terminates a frame immediately and does not require a FCS or an ending flag.

An abort pattern followed by a minimum of eight additional consecutive ones idles the data link. Thus, seven to fourteen ones establish the abort pattern; fifteen or more ones constitute an idle pattern.

Interframe time fill is accomplished by transmitting continuous flags. Therefore, the transmitter must be capable of sending multiple flags to maintain the active state in the receiver if any time fill is required.

4.2. IMPLEMENTATION

A representation of the HDLC process is shown in Figure 4-3. The events are numbered in order of occurrence from one to four.

1. The beginning flag is transmitted. The receiver sees the flag and now becomes aligned with the transmitter. Both the receive and the transmitter FCS registers are preset to FFFF (hex).

2. The information field is transmitted. The data is also run through the FCS register before zero insertion. At the receive end, after the zero deletion algorithm, the data is presented to the user and then run through the FCS register.

3. The FCS is inverted and then transmitted. The transmitted FCS is passed through the receiver's FCS register. The shift register will contain 1111000010111000 if the frame has been received correctly.

4. The ending flag is transmitted.

TRANSMITTER AND RECEIVER SETUP

In order to use HDLC in the modem, the host must:

1. Set up the modem configuration.

2. Set the Transmitter Parallel Data Mode bit (TPDM). Received data is always available in parallel.

3. Switch into synchronous mode by resetting the ASYNC bit, if not already in synchronous mode.

4. Set the SYNCMD bits for SDLC/HDLC mode (01).

Note: The host should enter into SDLC/HDLC mode only after the handshake is complete.

HDLC transmission cannot be performed using the serial interface. The format of the data input to the modem is in groups of 8-bit bytes. As in the normal synchronous parallel data mode, the least significant bit of the byte is transmitted first.

TRANSMISSION AND RECEPTION RATE

The HDLC as implemented in the modem can be used in all transmitter and receiver data modes except the FSK modes.

FLAG TRANSMISSION AND RECEPTION

Once in HDLC mode, the modem will send continuous flags with no zero sharing (i.e., 0111111001111..) until the user loads data into the transmit data buffer TBUFFER (register 10). Thus, the transmitter defaults to transmitting time-fill and keeps the receiving link station active. The status bit FLAGS (0F:0) indicates that the modem is transmitting the flag sequence.

When in HDLC mode, the modem receiver continually searches for the flag data pattern. When one or more flags are detected, status bit SYNCD (0F:1) is set. The flags themselves are not presented to the host through the receiver data buffer RBUFFER (register 00).

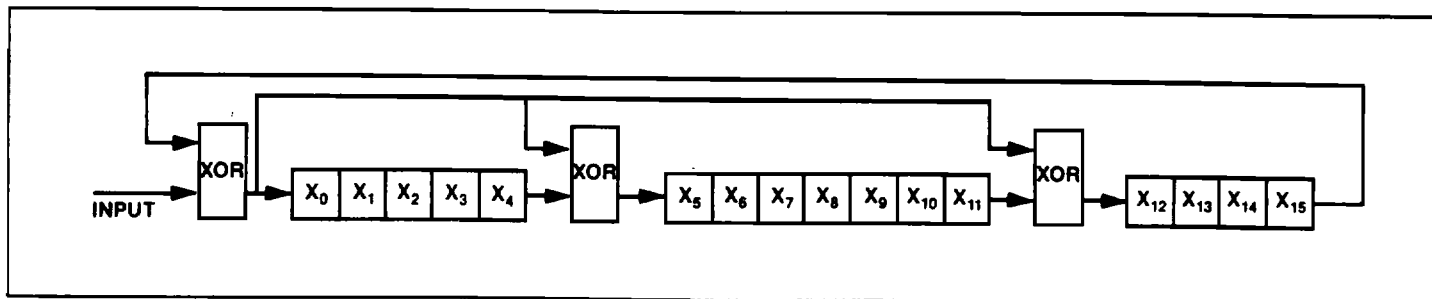The modem also has the capability to detect consecutive flags with zero-sharing.

Figure 4-2. CRC Polynominal Inplementation

INFORMATION FIELD TRANSMISSION AND RECEPTION

The host must load the data into TBUFFER and then wait for the Transmit Data Buffer Available bit TDBE (1E:3) to be set by the modem before loading in the next byte of data. If the next byte is not loaded into TBUFFER within the next eight bit times, the modem interprets this as the end of a frame and sends the CRC sequence.

In the receiver, data between flags is passed to the host through the RBUFFER register by the use of the hand-shaking bit RDBF (1E:0). The host must wait for RDBF to be set by the modem and then take the data. If the host does not read the data within eight bit times, the data in RBUFFER will be overwritten by the next byte and the Overrun Error bit (0E:3) will be set. The flag sequence and abort/idle sequence are not presented to the user. The receiver determines where the FCS field is by detecting the ending flag. There is at least a 16-bit time delay in the reception of data.

FCS AND ENDING FLAG TRANSMISSION AND RECEPTION

Following the detection of no new data loaded into the TBUFFER register within the next eight bit times, the modem automatically sends the FCS and ending flag. Status bit CRCS (0A:0) in the interface memory is set just before the highest order bit (x^{15}) is sent to indicate that the FCS is being transmitted. Once the host sees this bit set, the first byte of the next frame can be loaded. In this case, the ending flag serves as the beginning flag for the next frame. The CRCS bit is reset when the ending flag is transmitted. At the same time, the FLAGS bit is set.

Upon the receipt of an ending flag in the current frame (which may also be the beginning flag of the next frame), the receiver checks the data in the FCS register. If the FCS register remainder is correct, the PE bit (0E:5) is left a zero. If the remainder is incorrect, the PE bit is set. The FCS field is also passed to the host, in case the host wishes to do his own CRC checking. The receiver will set the SYNCD bit and the PE bit (if the modem detected a frame with a bad CRC) after sending the FCS to the host. The modem does not change the PE bit until the end of the next frame when a correct or incorrect frame is deter-
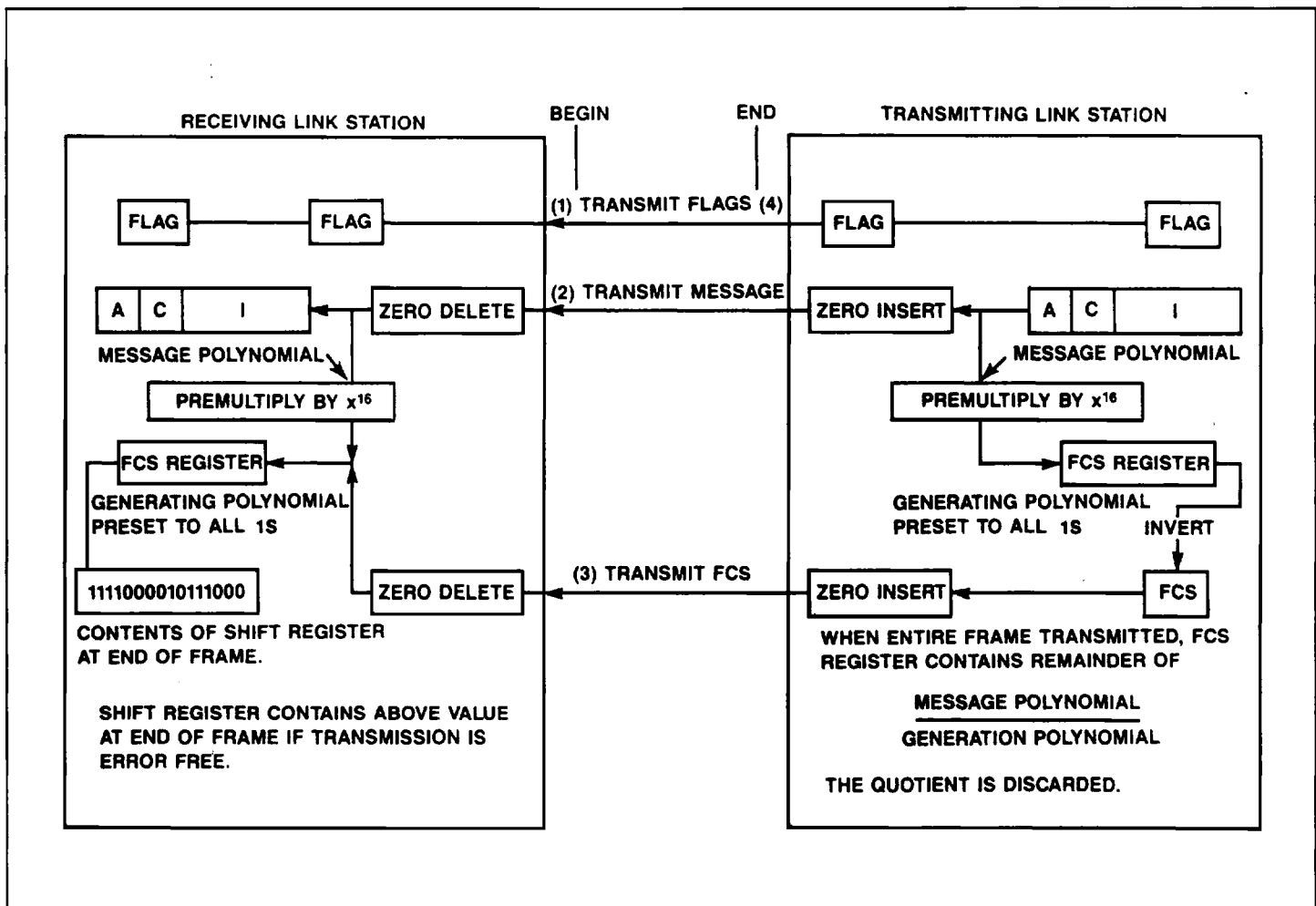

Figure 4-3. HDLC Process

mined. However, the host can reset this bit anytime. The modem presets the FCS register to all ones after one or more flags are received.

After the FCS transmission (immediately following bit x^0), one flag is sent to signify the end of the current frame and the beginning of the next frame. After the final zero in a flag is transmitted, the modem looks to see if the host has loaded new data into TBUFFER. If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag between frames is desired, the host must wait N-1 multiples of eight bit times after FLAGS is set by the modem to load new data into TBUFFER, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times and not more than 23 bit times after FLAGS is set by the modem.

ABORT/IDLE SEQUENCE TRANSMISSION AND RECEPTION

An abort/idle sequence can be sent by the host setting the MHLD bit (07:0) in the interface memory. This stops any normal frame transmission, as well as continuous flag transmission, and sends continuous ones. After the setting of MHLD is detected, the modem first completes the transmission of the current byte of data. Immediately after this transmission, the modem sends seven consecutive ones. After these seven bit times, if MHLD is still set, the modem continues to send ones until MHLD is reset. To discontinue this sequence, MHLD must be reset. Then, if no new data is loaded into TBUFFER, continuous flags are sent. If new data is loaded into TBUFFER, the modem sends a beginning flag and then the data in TBUFFER.

The modem receiver not only continually searches for flags, but also continually searches for an abort/idle sequence. When the receive modem encounters this data pattern, it sets the FE bit (0E:4). After the modem sets the FE bit, it does not change the bit until the end of the next frame when the abort/idle sequence is again determined. However, the host can reset the FE bit anytime. Then, if an abort/idle sequence is detected during the next frame, the modem will again set the FE bit. The reception of data following the abort/idle sequence is treated as invalid data and is not presented to the host. Therefore, to re-establish transmitter and receiver synchronization, the receiver must see at least one flag. Remember, the abort/idle sequence is not output through the RBUFFER register.

4.3. EXAMPLE APPLICATION

Refer to Table 3-1 for a description of the bits associated with the HDLC functions. Figure 4-4 illustrates the timing of these bits.

TRANSMITTER EXAMPLE

1. After handshake, reset the ASYNC bit. Then set the SYNCMD bits for SDLC/HDLC and set RTS.

2. The modem starts transmitting flags immediately and continues with flags until the first byte of data is loaded into TBUFFER.

3. Place the first byte of data into TBUFFER. The modem finishes transmitting the current flag followed by this byte of data.

4. As soon as TDBE is set, load in the next byte of data. This must occur within eight bit times of TDBE being set.

5. After all information but the last byte is given to the modem, load in the last byte of data in the frame as in step 4.

6. Wait until CRCS is reset to load in the first byte of the next frame. The modem follows the last byte of the current frame with the 16-bit FCS and a flag.

7. Repeat steps 4 through 6 for all frames to be transmitted.

RECEIVER EXAMPLE

The steps to perform a typical HDLC reception are:

1. After handshake, reset the ASYNC bit. Then monitor, through interrupts, the RDBF, OE, SYNCD, PE and FE bits in the interface memory.

2. Wait for an interrupt. If it is caused by the modem setting RDBF (RDBIA is also set by the modem), read the data in RBUFFER. The modem will set the NEWS and NSIA bits if any of the other bits caused the interrupt. An interrupt caused by OE indicates that RBUFFER was loaded with new data before the host read the old data. SYNCD indicates that the modem is receiving flags. PE indicates that the FCS had an incorrect CRC. FE indicates that an abort/idle sequence is detected, and the frame that was aborted is invalid. The modem does not set the SYNCD bit or the PE bit in this case since no FCS checking is done.

3. Continue waiting for interrupts and take appropriate action when the interrupts are received.
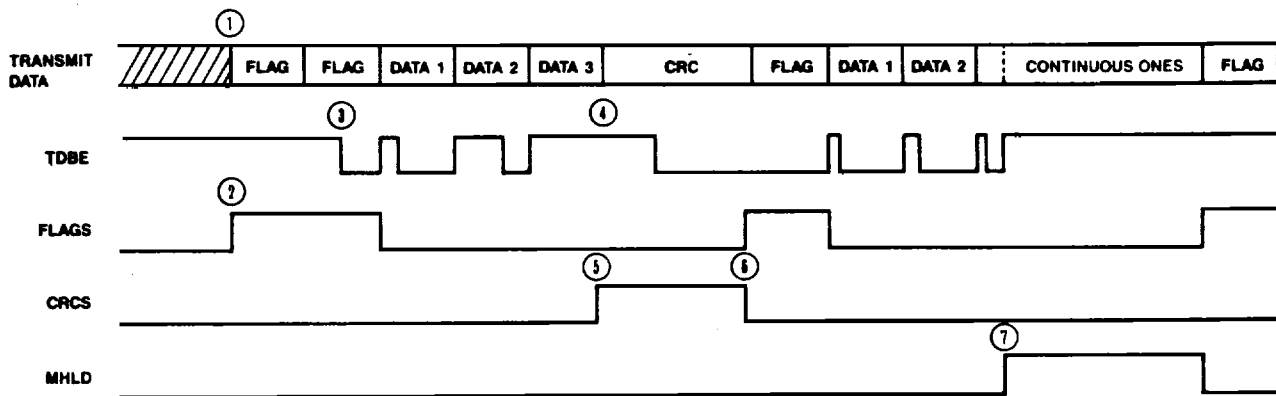
1. The host enters HDLC mode by setting SYNCMD = 01 after a connection is established.

2. The modem sets FLAGS prior to sending the first bit of the first 7E flag.

3. If the host loads the first data byte into TBUFFER while FLAGS is being sent, the data will not be sent until the flag is completely sent.

4. After TDBE is set, the host has 8 bit times to load new data into TBUFFER.

5. CRCS is set as soon as the last bit of the last data byte is sent and prior to sending the first bit of the CRC sequence. As soon as CRCS is set, a new data byte of the next frame can be loaded.

6. CRCS is reset and FLAGS is set when the last bit of the CRC sequence is sent.

7. If MHLD is set anytime during the data, CRC, or flag transmission, the byte transmitted is interrupted and the abort sequence is started.

a. Transmitter
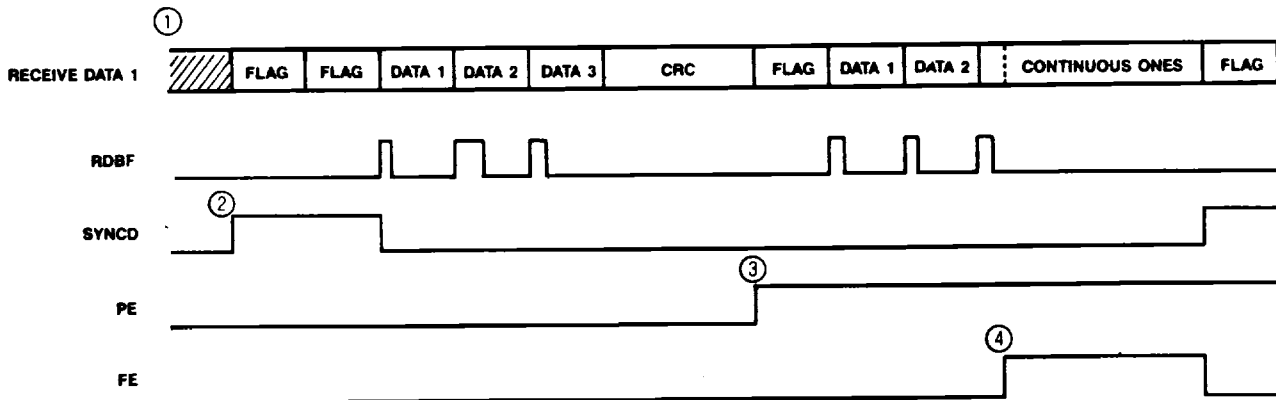
1. Timing refers to when received data is presented to the host. Flags and the abort sequence are not presented to the host.

2. SYNCD will turn on 8-15 bit times after entering SDLC/HDLC mode, when 7E flags are detected.

3. PE is set only if a bad CRC is detected by the modem.

4. FE will turn on when seven consecutive 1s are detected.

b. Receiver

Figure 4-4. HDLC Signal Timing

5. TONE DETECTOR FILTER TUNING

This section describes a method of tuning the filters in the modem for tone detection. The modem includes four independently programmable filters in Dial/Call Progress mode, three filters in Tone Generation mode, and three filters in Handshake mode. Handshake mode occurs when the modem is configured for V.22 bis or V.22, DATA = 1, LL = 0, and RLSD = 0. Consult Diagnostic Data Scaling in Section 3 for the RAM addresses corresponding to each filter. Table 3-3 shows which status bits, tone detect threshold, and Tone Power addresses correspond to each filter in each mode.

Status bit TONEA in Call Progress mode represents the output of two cascaded second-order biquadratic filters. The default frequency response of this filter is shown in Figure 5-5. This filter can be used to detect a range of call progress tones. All other status bits represent single second-order biquadratic filters. This section presents a method of tuning the call progress filter to any range in the 400 Hz-3 kHz band.

Note: When reconfiguring from Dial/Call Progress mode to Tone Generation/Detection mode, the host must first configure the modem for V.22 bis mode (CONF = 84) to initialize the tone detect filters.

5.1. COMPUTATION OF TONE DETECTOR COEFFICIENTS

The call progress tone filter (TONEA) consists of two second-order filters in cascade, an energy averaging filter and a threshold comparator. A diagram of the tone detector is shown in Figure 5-1.

Filter 1 has a transfer function:

$$H_1(Z) = \frac{2(\alpha_0 + \alpha_1 Z^{-1} + \alpha_2 Z^{-2})}{1 - 2\beta_1 Z^{-1} - 2\beta_2 Z^{-2}} \quad \text{(Eq. 1)}$$

Filter 2 has a transfer function:

$$H_2(Z) = \frac{2(\alpha'_0 + \alpha'_1 Z^{-1} + \alpha'_2 Z^{-2})}{1 - 2\beta'_1 Z^{-1} - 2\beta'_2 Z^{-2}} \quad \text{(Eq. 2)}$$

The energy averaging filter has a transfer function:

$$H_3(Z) = \frac{\alpha''}{1 - \beta'' Z^{-1}} \quad \text{(Eq. 3)}$$

The output of the energy averager is fed to a threshold comparator that sets interface memory bit TONEA if the output is equal to or greater than 1/8 of full scale, otherwise, the bits are reset.
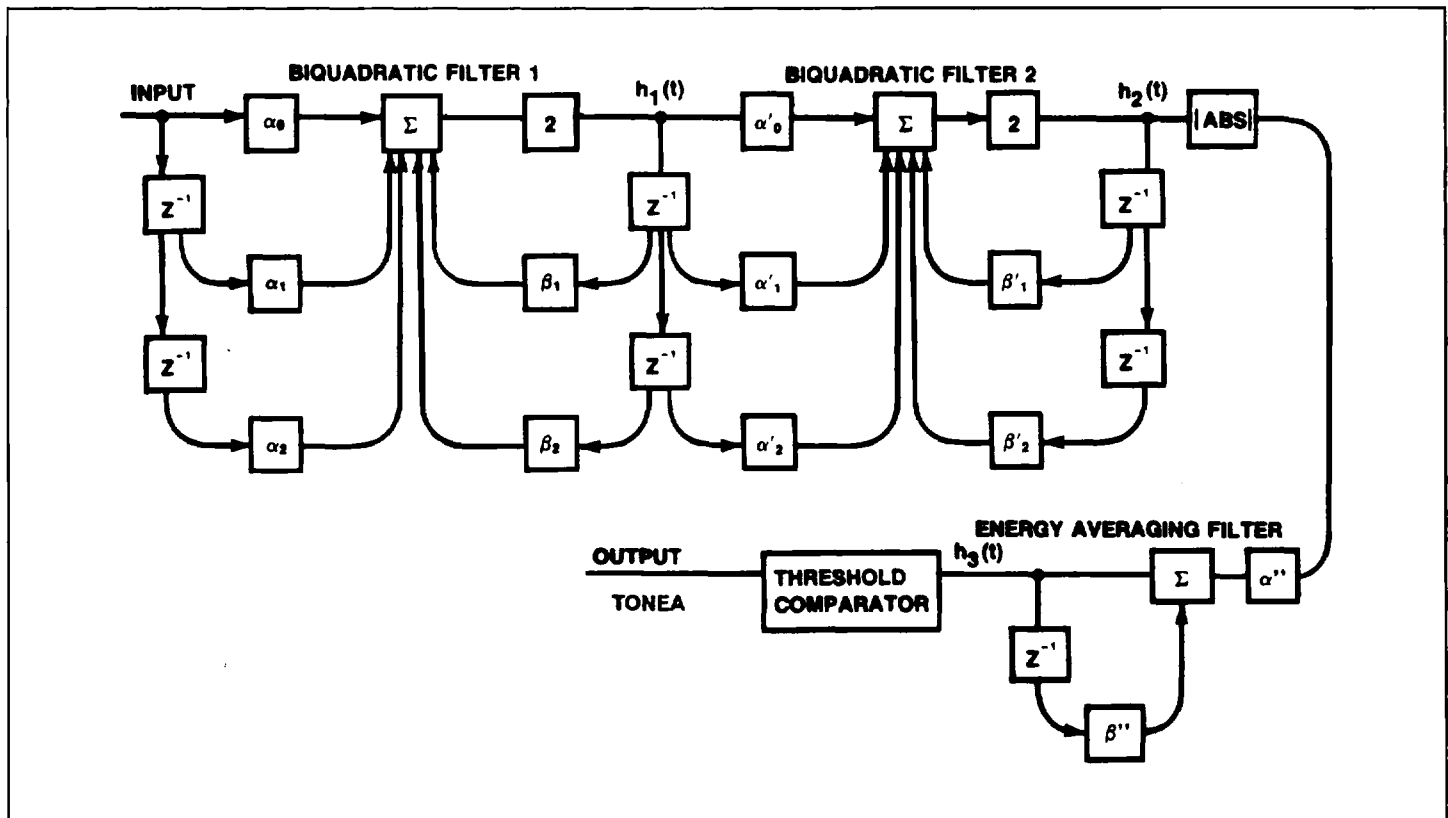

Figure 5-1. Modem Tone Detection Diagram

Given the transfer functions $H_1(Z)$ and $H_2(Z)$, an analytical method is required to compute their coefficients for any frequency in the 400 Hz – 3 kHz band. First, consider $H_1(Z)$. This transfer function can be rewritten as:

$$H_1(Z) = \frac{2(\alpha_0 Z^2 + \alpha_1 Z + \alpha_2)}{Z^2 - 2\beta_1 Z - 2\beta_2} \qquad \text{(Eq. 4)}$$

which has a conjugate pair of poles:

$$P_1 = \beta_1 + j\sqrt{(\beta_1^2 + 2\beta_2)}$$

and

$$P_2 = \beta_1 - j\sqrt{(\beta_1^2 + 2\beta_2)}$$

Upon power up, these poles lie on a circle of radius 0.994030884 on the Z-plane. The radius of the tone detector circle was chosen so that each filter has a high Q without being unstable (i.e., poles must lie inside the unit circle for stability). Figure 5-2 shows a Z-plane pole-zero diagram for an arbitrary conjugate pole pair on the tone detector circle. The angle $\theta = 360° \ f_O/f_S$, where f_O is the desired center frequency and f_S is the sampling rate (f_S = 7200). In this design, a double zero is placed at the origin. This is obtained by setting $\alpha_1 = \alpha_2 = \alpha'_1 = \alpha'_2 = 0$. A more sophisticated filter design may be used to place zeros using α_1, α_2, α'_1, and α'_2.

The following equations are derived from the angle and magnitude of the position vector pointing to a pole pair located at the desired angle:

$$\cos^{-1}(\beta_1/r) = \theta = 360° \times f_O/f_S \qquad \text{(Eq. 5)}$$

$$\sqrt{[\beta_1^2 + (-\beta_1^2 - 2\beta_2)]} = r = 0.994030884 \quad \text{(Eq. 6)}$$

Solving for β_1 and β_2:

$$\beta_1 = r \cos (360° \times f_O/f_S) \qquad \text{(Eq. 7)}$$

$$\beta_2 = -r^2/2 \qquad \text{(Eq. 8)}$$

In deriving these equations, only $H_1(Z)$ was considered. However, the tone detector consists of two identical filters in cascade. Shifting filter 1 and filter 2 above and below the desired center frequency, a response with the desired bandwidth is achieved. α_0 controls the amplitude response, and one may set $\alpha_0 = \alpha'_0$ to uniformly raise or lower the overall cascade response.

From Equation 8, we see that:

$$\beta_2 = \beta'_2 = -r^2/2 = -0.494048699$$

Rewriting Equation 7 in terms of the offsets f_A and f'_A we obtain:

$$\beta_1 = r \cos [360° \ (f_O - f_A)/f_S] \qquad \text{(Eq. 9)}$$

$$\beta'_1 = r \cos [360° \ (f_O + f'_A)/f_S] \qquad \text{(Eq. 10)}$$

The frequency offset is approximately 72% of B/2 (half the bandwidth) for most applications:

$$f'_A \approx 0.72 \ (B/2) \qquad \text{(Eq. 11)}$$

The value of f_A should be equal to f'_A. However, f_A may be chosen 1% smaller than f'_A to compensate for the fact that the overall cascade response is not perfectly symmetrical, i.e., near D.C. (see Figure 5-3).

The values for the coefficients α_0 and α'_0 that set $|H(f_O)|$ = 0 dB in equations 1 and 2 were measured and plotted versus center frequency f_O as shown in Figure 5-4. Three equations corresponding to three linear approximations result:

$$\alpha_0 = \alpha'_0 = \frac{(104/319)f_O - 78.62}{32767}$$
$$400 \leq f_O \leq 1100 \text{ Hz} \qquad \text{(Eq. 12a)}$$

$$\alpha_0 = \alpha'_0 = \frac{(44/275)f_O + 104}{32767}$$
$$1100 \leq f_O \leq 1650 \text{ Hz} \qquad \text{(Eq. 12b)}$$

$$\alpha_0 = \alpha'_0 = \frac{(4/45)f_O + 221}{32767}$$
$$1650 \leq f_O \leq 3000 \text{ Hz} \qquad \text{(Eq. 12c)}$$

The call progress filter default response is shown in Figure 5-5.

5.2. ENERGY AVERAGING FILTER

The coefficients of the energy averaging filter are determined by a Z-domain approximation to an RC circuit of transfer function $H(S) = 1/1 + S\tau$.

$$\alpha'' = \frac{1}{1 + f_S\tau} \qquad \text{(Eq. 13)}$$

$$\beta'' = \frac{1}{(1 + 1/f_S\tau)} \qquad \text{(Eq. 14)}$$

Upon power up, α'' and β'' are set for τ = 0.1 seconds. These values can not be changed by the host.
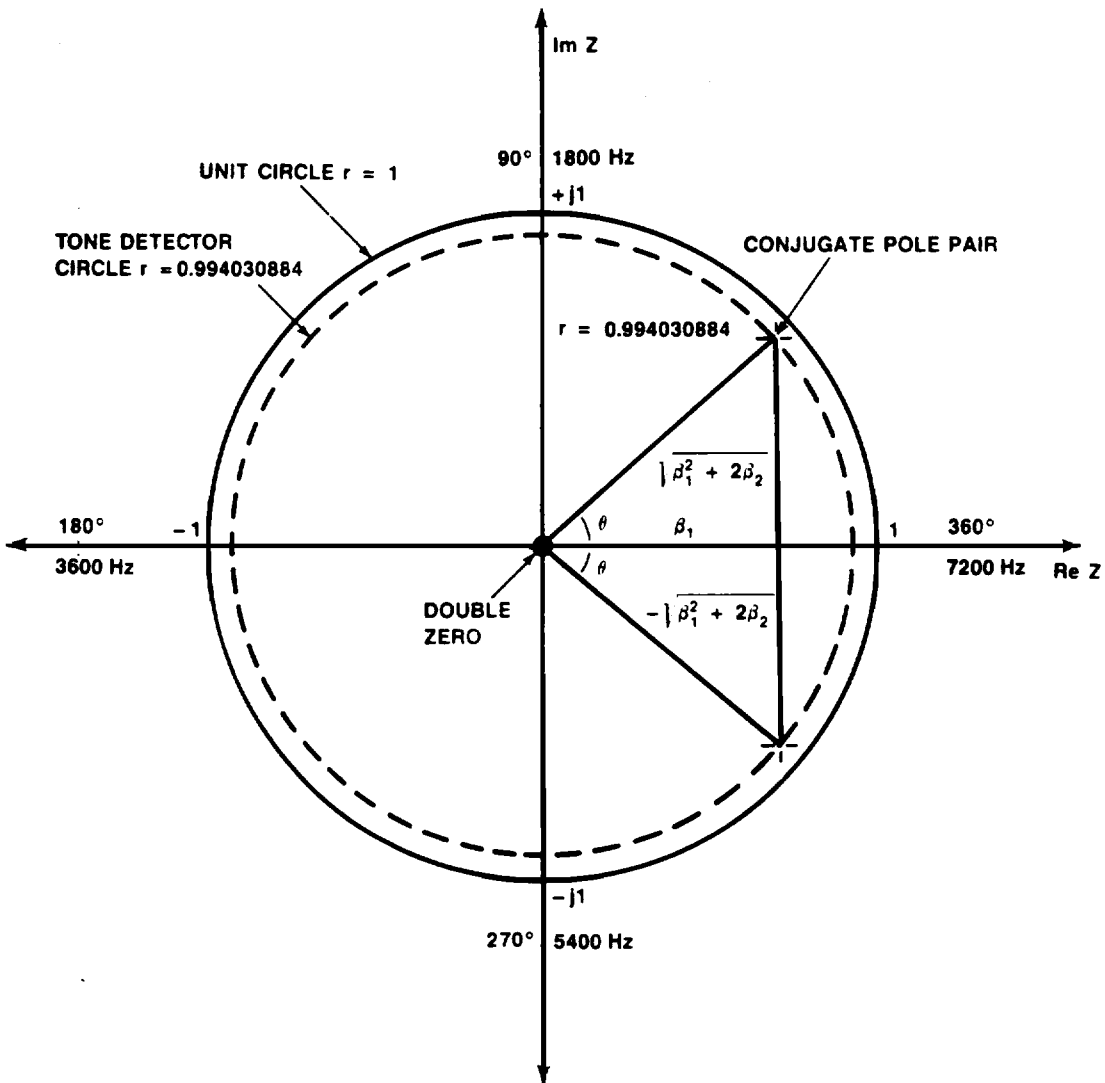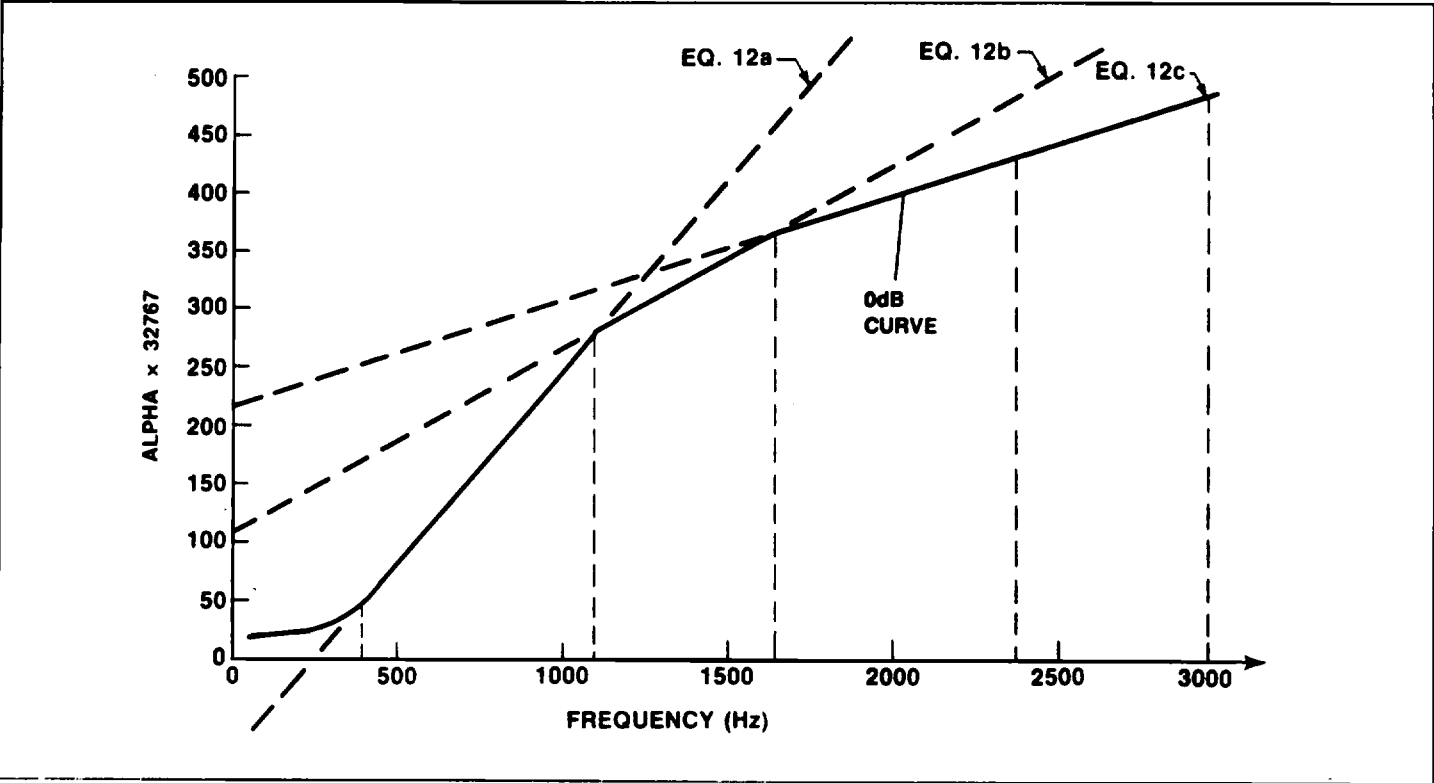
Figure 5-2. Z-Plane Pole-Zero Diagram
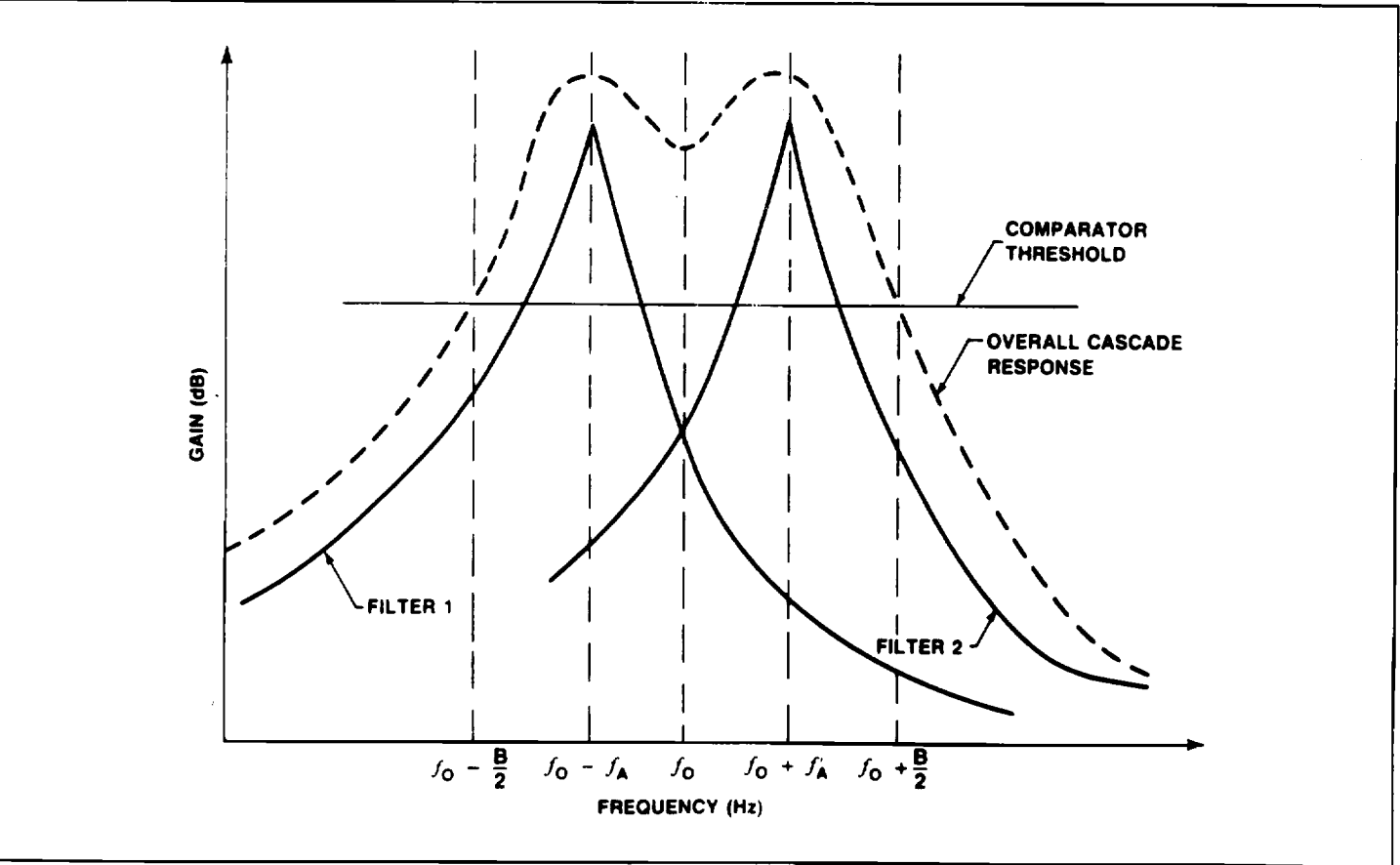
Figure 5-3. Bandwidth and Offset Frequencies
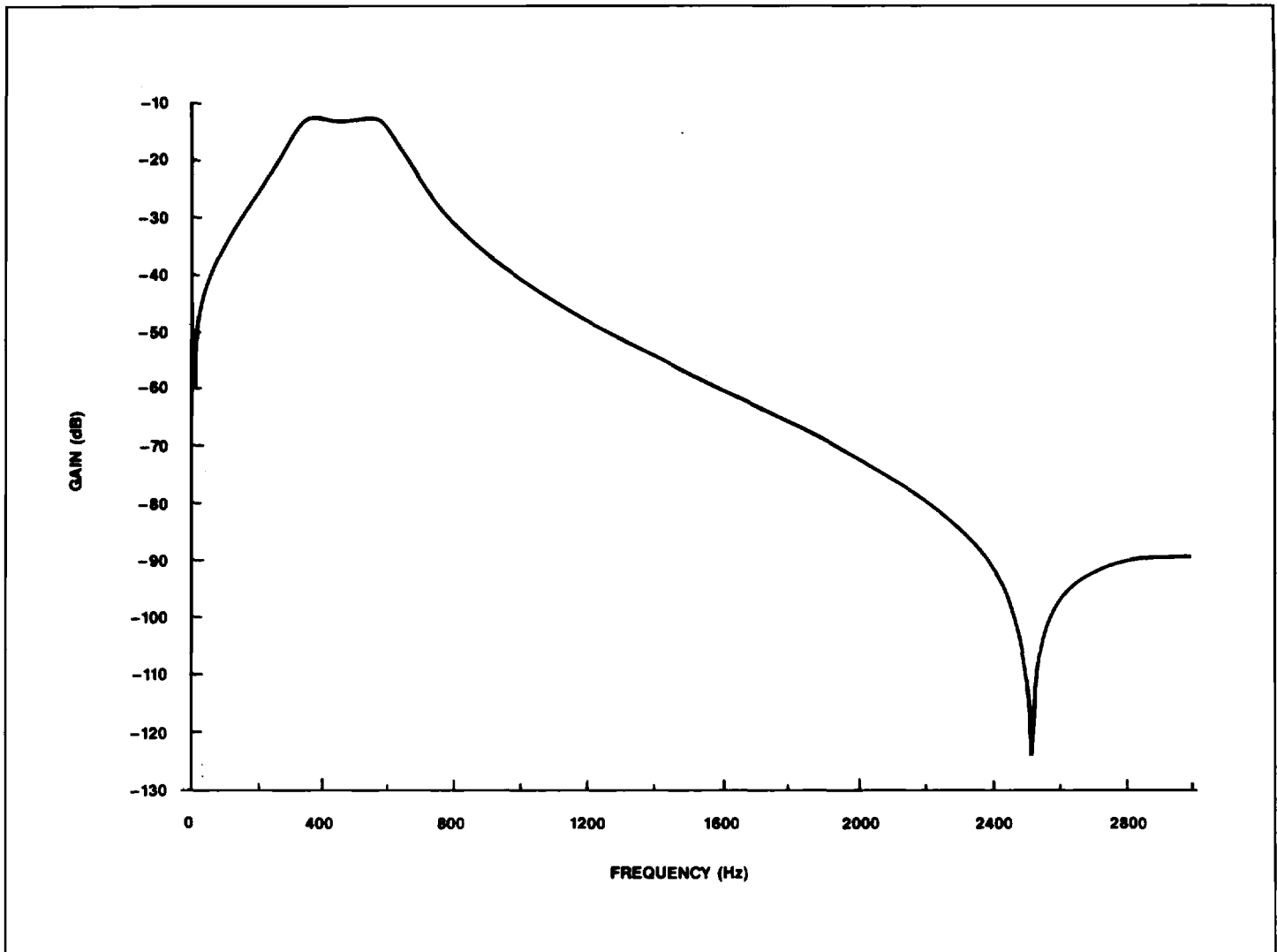

Figure 5-4. Alpha-zero Center Frequency

Figure 5-5. Frequency Response of Call Progress IIR

6. HANDSHAKING

6.1. V.22/V.22 bis HANDSHAKING PROCEDURES

CCITT recommendations V.22 and V.22 bis define operation on both the GSTN and two-wire point-to-point leased circuits. The means for obtaining synchronization for both modes is described in this section.

6.1.1. Point-to-Point Leased Circuits (Controlled Carrier)

Once an ON condition has been applied to $\overline{\text{RTS}}$ by the DTE, the modem transmits a synchronizing signal corresponding to binary 1 applied to TXD. The ON condition is applied to $\overline{\text{CTS}}$ 210 to 275 ms after starting to transmit the synchronizing signal. The receiving modem establishes timing and descrambler synchronization and then turns $\overline{\text{RLSD}}$ ON in 40 to 65 ms.

6.1.2. GSTN Handshake Sequence

The means of achieving synchronism between the calling modem and the answering modem on GSTN connections is shown in Figures 6-1 through 6-6. Both calling and answering modems may be conditioned to operate either in the synchronous modes or in the start-stop modes. If both calling and answering modems are V.22 bis modems, the handshake will normally condition both modems to operate at 2400 bps. If, however, one or both of the modems has been set to operate at 1200 bps, then the handshake will condition both modems to operate at 1200 bps. The signaling rate is communicated to the DTE by the SPEED bits in the interface memory. The handshake sequence is independent of whether the calling or answering modem is connected to the line first. Figure 6-7 shows a Bell compatible 2400 bps handshake which is also implemented when the modem is the originate modem. It is identical to V.22 bis 2400 bps except the 2225 Hz replaces 2100 Hz and unscrambled ones sequence.

The V.25 automatic answering sequence is transmitted from the answer modem on GSTN connections. The V.25 answer sequence can optionally be selected off by setting the NV25 bit (09:7). The transmission of the sequence is omitted in connections on point-to-point leased circuits.

The host should select the leased line mode by setting the LL bit (and the NEWC bit) after handshake is completed in switched line mode. This sequence allows incorporation of a carrier recovery algorithm in leased line mode.

INTERWORKING AT 2400 BPS V.22 bis

Calling Modem

1. On connection to line, the calling modem receives signals in the high channel and is ready to transmit signals in the low channel. The modem turns on $\overline{\text{DSR}}$ (circuit 107) but initially remains silent.

2. After 155 ±10 ms of unscrambled binary 1 has been detected, the modem remains silent for a further 456 ± 50 ms, then transmits an unscrambled repetitive double digit pattern of 00 and 11 at 1200 bps for 100 ± 3 ms (S1 sequence). Following this, scrambled binary 1s are transmitted at 1200 bps.

3. If the modem detects scrambled binary 1 in the high channel at 1200 bps for 270 ± 40 ms, the handshake continues in accordance V.22 A/B. However, if unscrambled repetitive double dibit 00 and 11 at 1200 bps is detected in the high channel, then at the end of receipt of this signal the modem turns ON circuit 112 (Data Signalling Rate Selector).

4. 600 ± 10 ms after circuit 112 has been turned on, the modem begins transmitting scrambled binary 1 at 2400 bps, and 450 ± 10 ms after circuit 112 has turned ON the receiver begins making 16-way decisions.

5. Following transmission of scrambled binary 1 at 2400 bps for 200 ± 10 ms, $\overline{\text{CTS}}$ is conditioned to respond to $\overline{\text{RTS}}$ and the modem is ready to transmit data at 2400 bps.

6. When 32 consecutive bits of scrambled binary 1 at 2400 bps have been detected in the high channel, the modem is ready to receive data at 2400 bps and applies an ON condition to $\overline{\text{RLSD}}$.
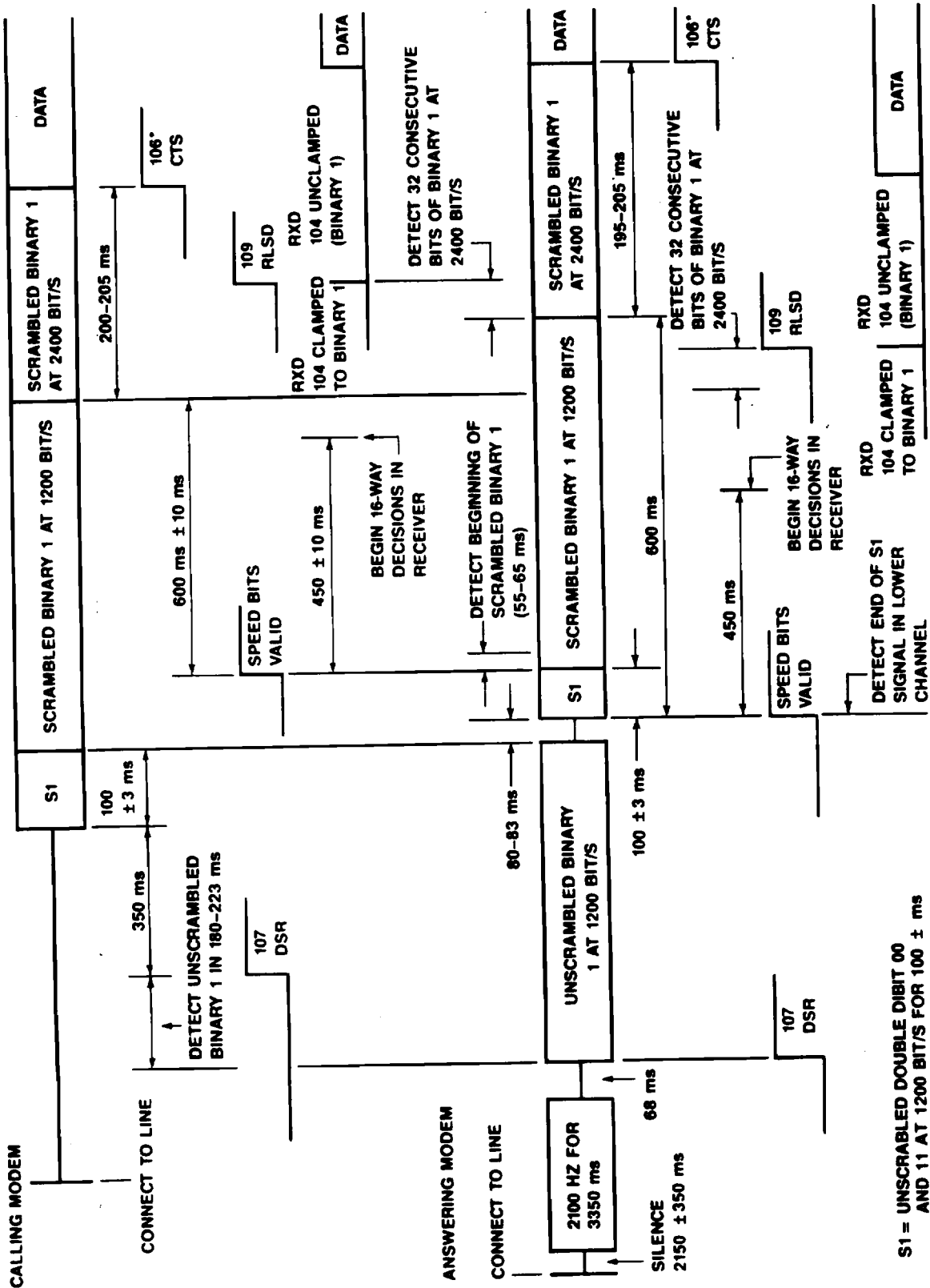
Answering Modem

1. On connection to the line, the answering modem transmits signals in the high channel and receives signals in the low channel. After the transmission of answer tone in accordance with V.25, the modem applies an ON condition to $\overline{\text{DSR}}$ and then transmits unscrambled binary 1 at 1200 bps.

2. If the modem detects scrambled binary 1 in the low channel at 1200 bps for 270 ± 40 ms, the handshake continues in accordance with V.22A/B. However, if unscrambled repetitive double dibit 00 and 11 at 1200 bps is detected in the low channel, at the end of receipt of this signal the modem turns circuit 112 ON and then transmits an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bps for 100 ± 3 ms (S1 sequence). Following these signals the modem transmits scrambled binary 1 at 1200 bps.
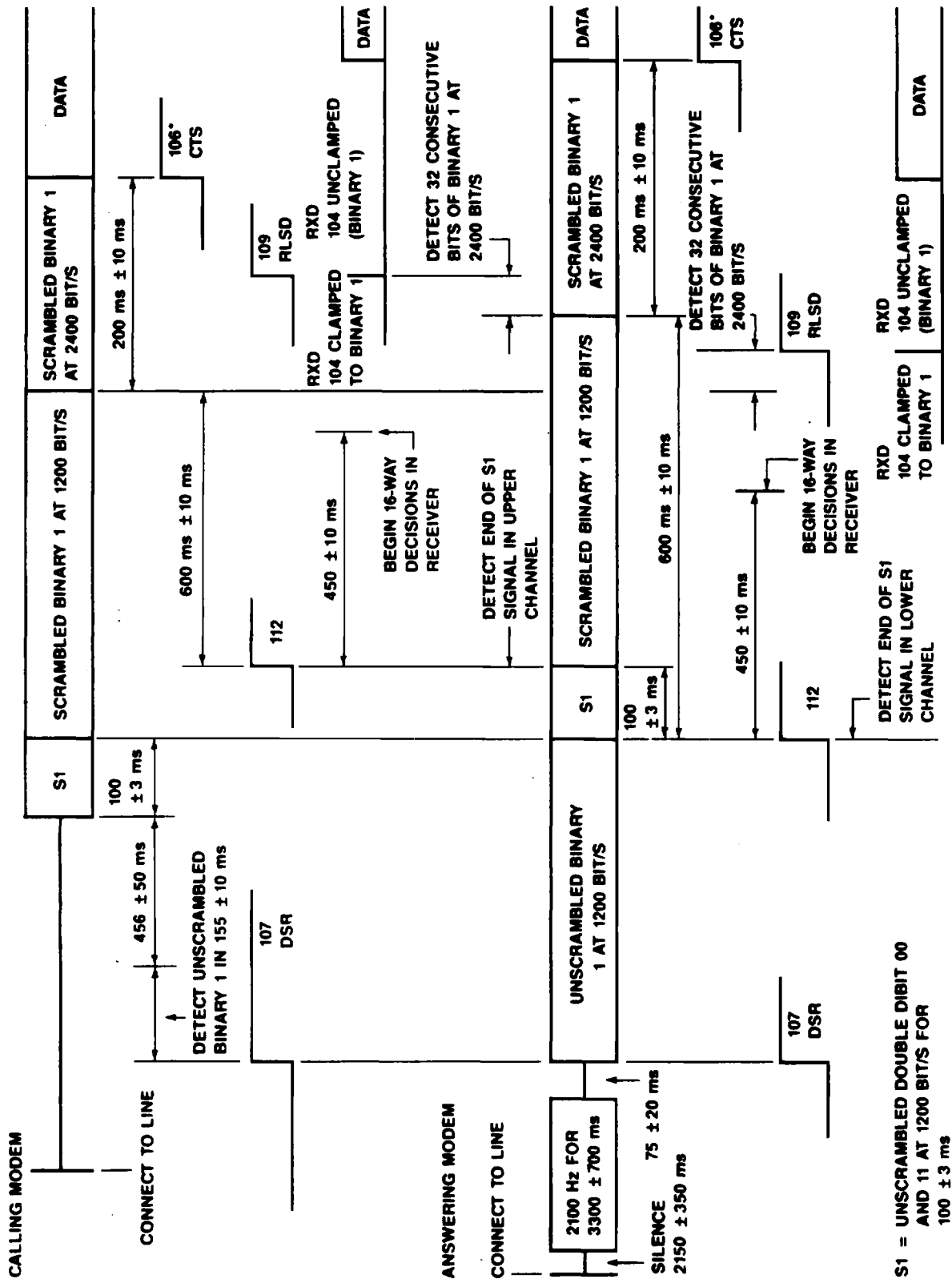
Figure 6-1. V.22 bis 2400 bps Connect Sequence - Std.

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Figure 6-2. V.22 bis 2400 bps Connect Sequence - Impl.

Figure 6-3. V.22 1200 bps Connect Sequence - Std.

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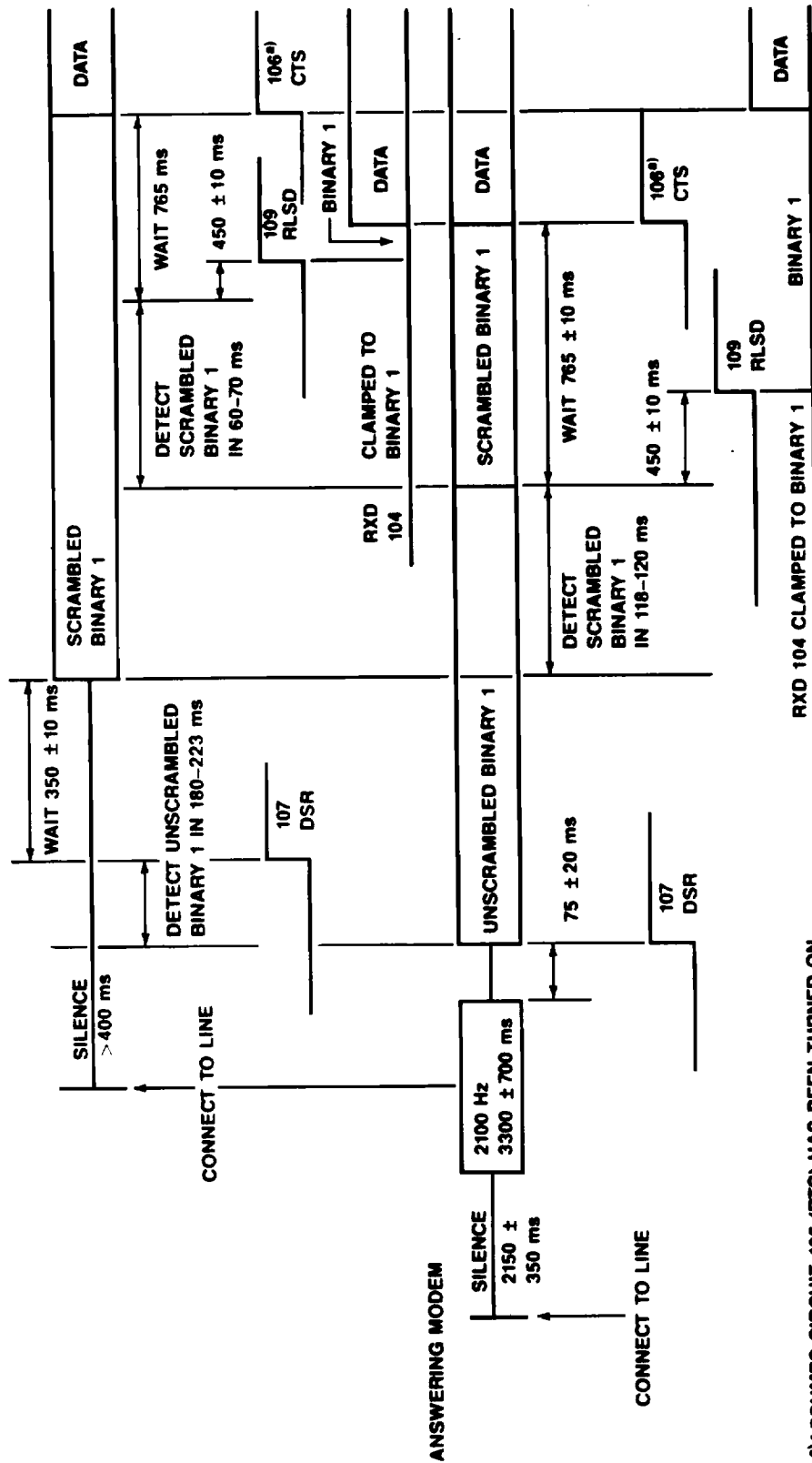
Figure 6-4. 1200 bps Connect Sequence - Impl.
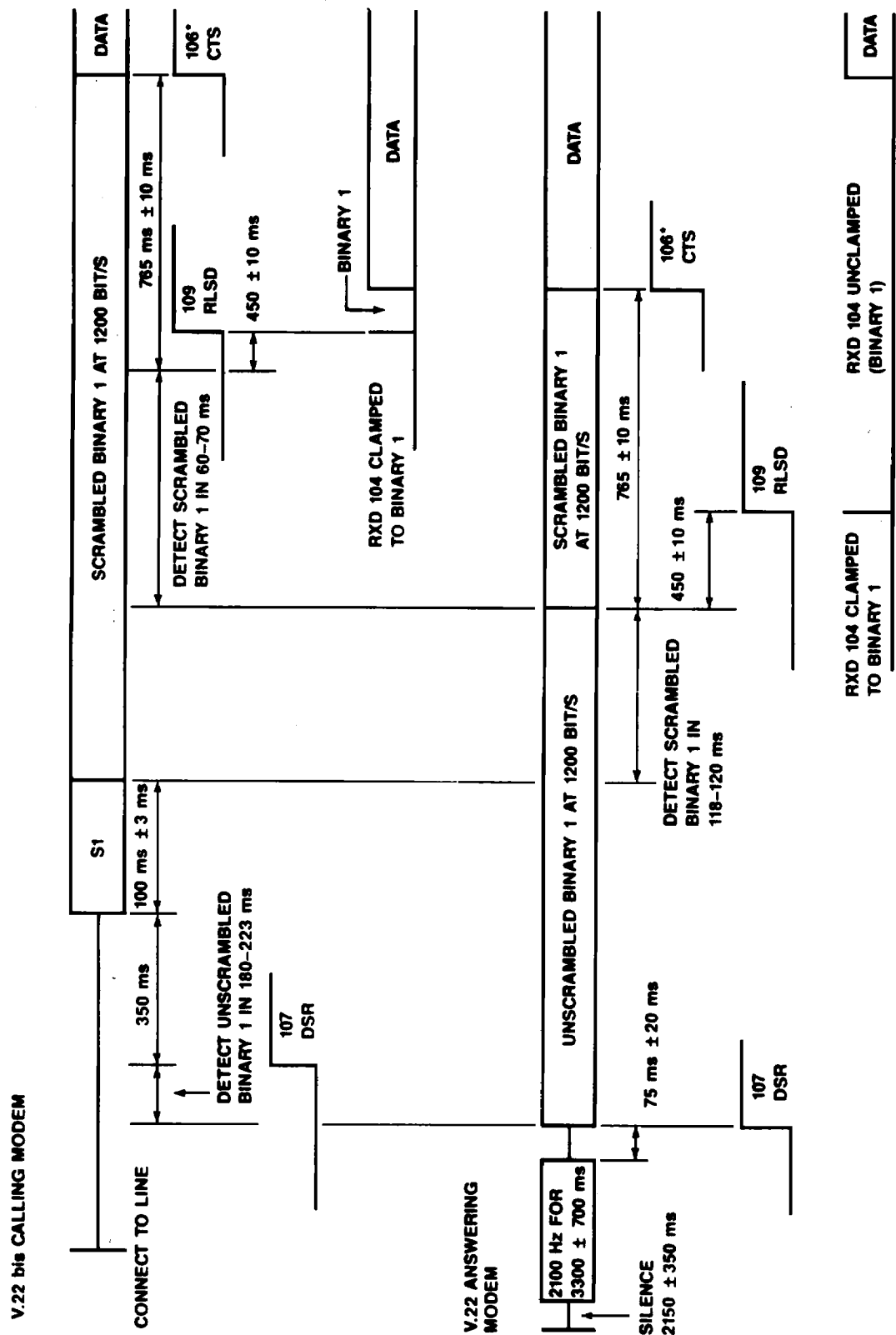
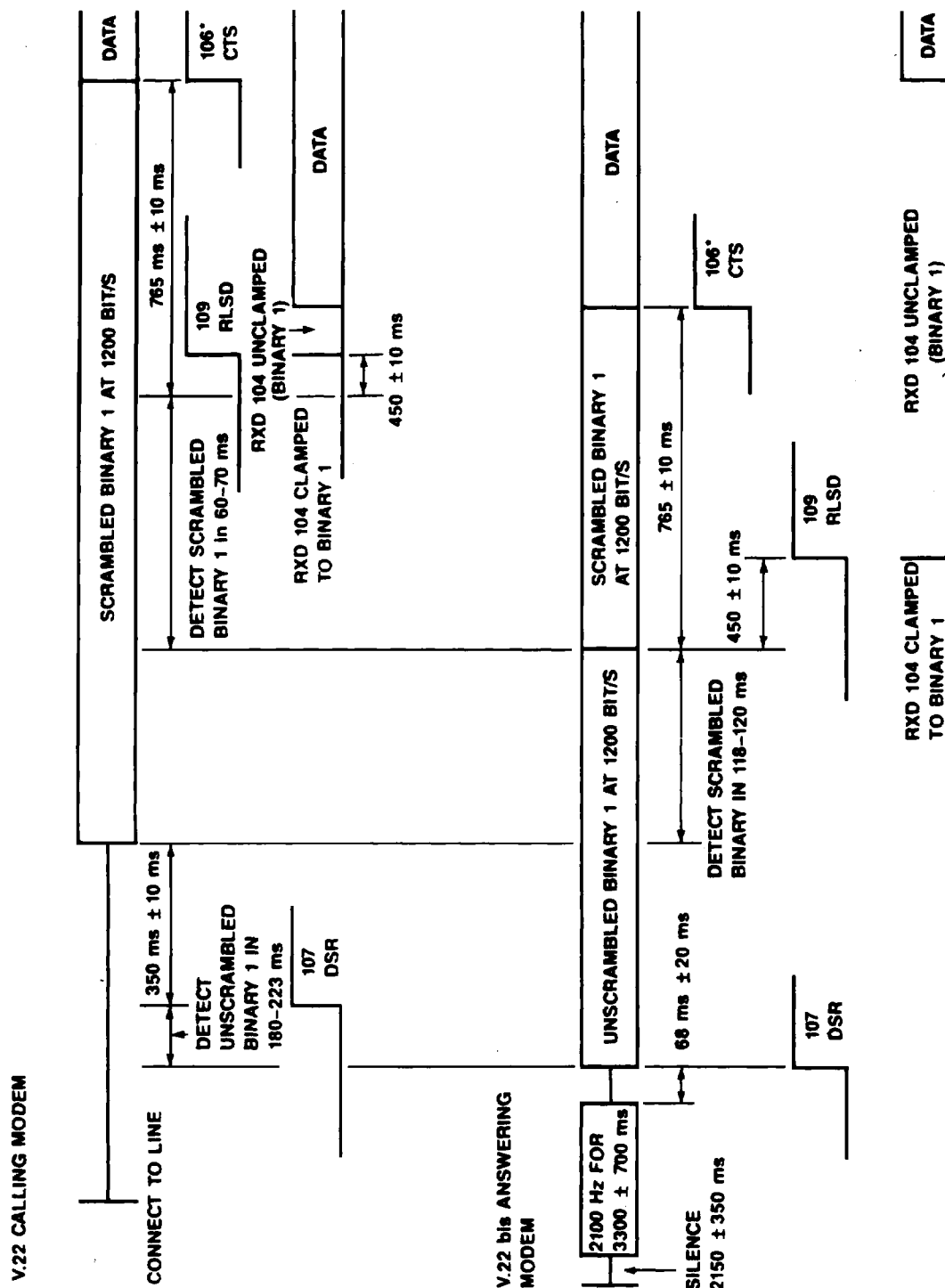Figure 6-5. 2400 bps Calling, 1200 bps Answering - Impl.

851C6

Figure 6-6. 1200 bps Calling, 2400 bps Answering - Impl.
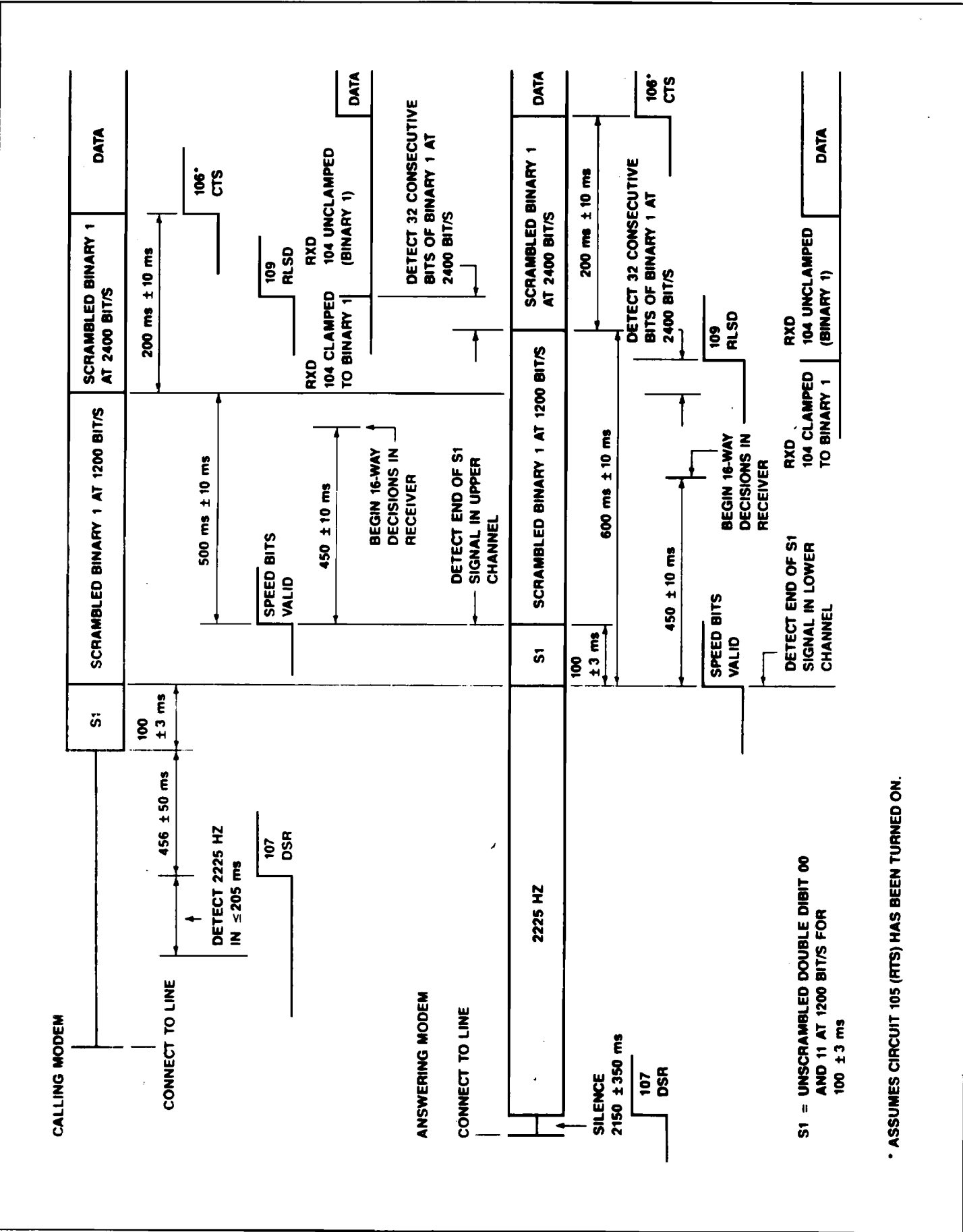
Figure 6-7. Bell Compatible 2400 bps Handshake - Impl.

851C6

3. 600 ± 10 ms after S1 has been detected the modem begins transmitting scrambled binary 1 at 2400 bps, and 450 ± 10 ms after circuit 112 has been turned ON the receiver begins making 16-way decisions.

4. Following transmission of scrambled binary 1 at 2400 bps for 200 ± 10 ms, CTS is conditioned to respond to RTS and the modem is ready to transmit data at 2400 bps.

5. When 32 consecutive bits of scrambled binary 1 at 2400 bps have been detected in the low channel, the modem is ready to receive data at 2400 bps and applies an ON condition to RLSD.

Modem Compliance with 2400 bps Connect Sequence.

The modem complies with the handshake interworking defined in V.22 bis with the deviations noted below. Handshake timing for V.22 bis recommendation and as implemented is shown in Figures 6-1 and 6-2, respectively.

1. Unscrambled mark is detected in 180-223 ms in the calling modem, at which time DSR turns on.

2. The amount of time to wait to transmit the S1 sequence in the calling modem is shortened to 350 ms to compensate for the late detection of unscrambled ones.

3. The modem indicates a data rate of 2400 bps by setting the SPEED bits in interface memory (0E:0-2) rather than turning circuit 112 ON.

4. The answer modem requires 80-83 ms to detect S1.

5. The answer modem detects the beginning of scrambled binary 1s in the upper channel rather than the end of the S1 sequence.

INTERWORKING AT 1200 BPS, V.22

Calling Modem

1. On connection to line, the calling modem receives signals in the high channel at 1200 bps and is ready to transmit signals in the low channel at 1200 bps. The modem turns ON DSR (circuit 107) but initially remains silent.

2. After 155 ± 10 ms of unscrambled binary 1s have been detected the modem remains silent for a further 456 ± 10 ms, then transmits scrambled binary 1 at 1200 bps (a preceding V.22 bis signal will not affect the operation of a V.22 answer modem).

3. On detection of scrambled binary 1s in the high channel at 1200 bps for 270 ± 40 ms, the modem is ready to receive data at 1200 bps and applies an ON condition to RLSD.

4. 765 ± 10 ms after RLSD has been turned ON, CTS is conditioned to respond to RTS and the modem is ready to transmit data at 1200 bps.

Answering Modem

1. On connection to line, the answering modem follows Recommendation V.25 by remaining silent for 2150 ± 350 ms, then sends 2100 Hz answer tone for 3300 ± 700 ms.

2. After transmitting answer tone, the answering modem transmits signals in the high channel at 1200 bps. The modem applies an ON condition to DSR and then transmits unscrambled binary 1 at 1200 bps.

3. On detection of scrambled binary 1s in the low channel at 1200 bps in 270 ± 40 ms, the modem transmits scrambled binary 1s at 1200 bps.

4. After scrambled binary 1s have been transmitted at 1200 bps for 765 ± 10 ms, the modem is ready to transmit and to receive data at 1200 bps, conditions CTS to respond to RTS and applies an ON condition to RLSD.

Modem Compliance with V.22 1200 bps Connect Sequence

The modem complies with the handshake interworking defined in V.22 with the deviations noted below. Handshake timing for V.22 recommendation and as implemented is shown in Figures 6-3 and 6-4, respectively.

1. Unscrambled mark is detected in 180-223 ms in the calling modem, at which time DSR turns on.

2. The amount of time to wait to transmit scrambled binary ones in the calling modem is shortened to 350 ms to compensate for the late detection of scrambled ones.

3. Scrambled binary ones are detected earlier in both the calling modem and the answer modem.

4. RLSD turns on 450 ± 10 ms after scrambled binary ones have been detected in both the calling and answering modem.

6.2. BELL 212A HANDSHAKING PROCEDURES

6.2.1. Bell 212A Handshaking Sequence

The Bell 212A handshaking sequence is designed to 100-series modem specifications when the modem is operated in the low-speed mode (Bell 103). In the high-speed mode (Bell 212), the events still occur in the same sequence except for an extra delay of approximately one second during the handshaking procedure. This is because extra time is required to acquire information in the high-speed mode of operation.

Specifically, the originating modem places a call to the answering modem which, upon receiving the call, places the modem (manually or automatically) into the data mode. In the data mode the channel is kept quiet for two seconds, then the transmitter (answering station) sends a 2225 Hz answer tone while the receiver listens to the low band for reply. The originating modem can be a 100-series modem or a 212A modem operating in the low-speed mode (Case A), or a 212A modem operating in the high-speed mode (Case B).

In Case A (low speed), the calling party detects the answer tone via the the telephone and places the modem into the data mode manually; or in the case of an automatically originated call, the originating modem automatically goes into the data mode. Once in the data mode, the originating modem waits 456 ± 10 ms to allow the disabling of echo suppressors, then sends a 1270 Hz tone (mark) for 756 ± 10 ms, and raises $\overline{\text{CTS}}$ to signal the customer to send data. The answering modem, upon detecting the low band mark decides it is talking with a 100-series modem, selects the low-speed mode of operation, and turns $\overline{\text{CTS}}$ and $\overline{\text{RLSD}}$ ON

In Case B (high speed), upon detecting the answer tone and waiting 456 ± 10 ms, the originating modem sends a low band mark in the form of a PSK signal through the transmitter scrambler (designated as scrambled mark). The answering modem requires ≤ 310 ms to detect scrambled mark after which the answering modem selects the high-speed mode of operation. The answering modem then terminates the 2225 Hz answer tone and transmits scrambled mark in the high band, waits 756 ± 10 ms to allow the originating modem to acquire timing information, and then raises $\overline{\text{CTS}}$ to the customer for data transmission. The originating data set requires ≤ 310 ms to detect scrambled mark, 450 ± 2 ms for the equalizer to adapt, then turns $\overline{\text{RLSD}}$ ON. The originating modem raises $\overline{\text{CTS}}$ 765 ± 10 ms after scrambled mark is detected.

The customer interface timing for high-speed and low-speed connect sequences are shown in Figures 6-7 through 6-11.

6.2.2. Modem Compliance with Bell 212A Connect Sequence

The modem is compatible with the Bell 212A connect sequence, with the deviations noted below. The timing for the high-speed standard and as implemented is shown in Figures 6-8 and 6-9, respectively. The timing for the low-speed standard and as implemented is shown in Figures 6-10 and 6-11, respectively.

High Speed (1200 bps)

1. In the originating modem, $\overline{\text{DSR}}$ turns ON 60-130 ms after detecting answer tone rather than 100-200 ms.

2. In the originating modem, $\overline{\text{RLSD}}$ turns ON 510-610 ms after P2M is being received. This allows the receiver adaptive equalizer to train.

3. In the answer modem, P1M is sent 120-130 ms after P1M is received instead of 231-308 ms. Also, $\overline{\text{RLSD}}$ turns ON 450 ms after P2M is sent instead of 774 ms.

4. In both the originate and answer modem, $\overline{\text{CTS}}$ turns ON 9 ms early.

Low Speed (300 bps)

1. In the originating modem, $\overline{\text{CTS}}$ turns on 853-856 ms after $\overline{\text{RLSD}}$, instead of 755-774 ms.

2. In the answer modem, $\overline{\text{CTS}}$ turns on 426 ms after $\overline{\text{RLSD}}$ turns ON, instead of turning ON concurrently with $\overline{\text{RLSD}}$.

6.3. V.21 HANDSHAKING PROCEDURES

CCITT Recommendation V.21 does not specify a handshake procedure. The modem handshake timing for this mode has been designed to be compatible with other V.21 modems. This timing is described in figure 6-12.

6.4. V.23 HANDSHAKING PROCEDURES

CCITT Recommendation V.23 does not specify a handshake procedure. The modem handshake timing for V.23 differs slightly depending on whether the modem is configured for 1200 bps half-duplex, 75 bps half-duplex, or asymmetric mode (1200 bps one direction, 75 bps in the opposite direction). The handshake timing for these modes is shown in Figures 6-13 through 6-15.
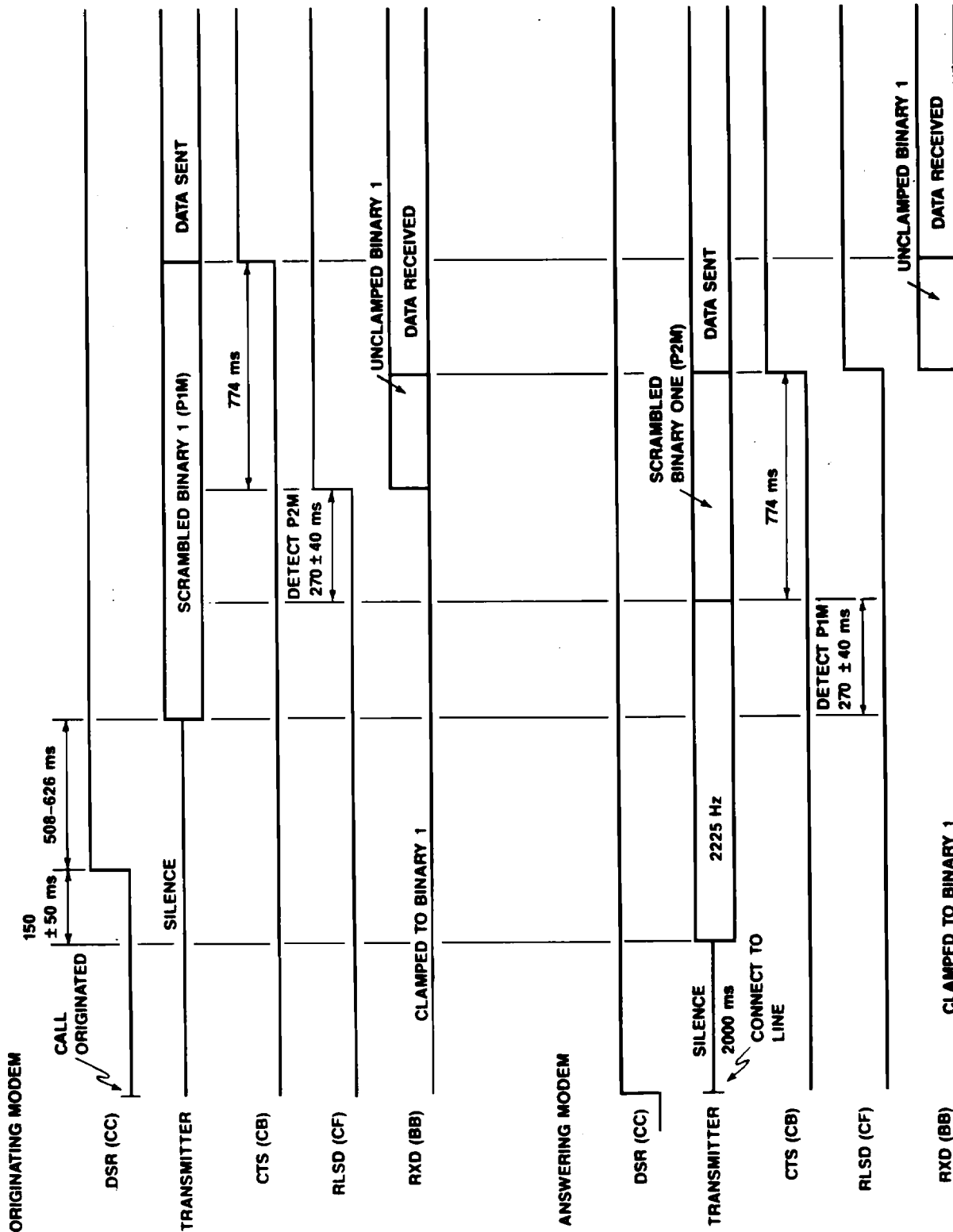
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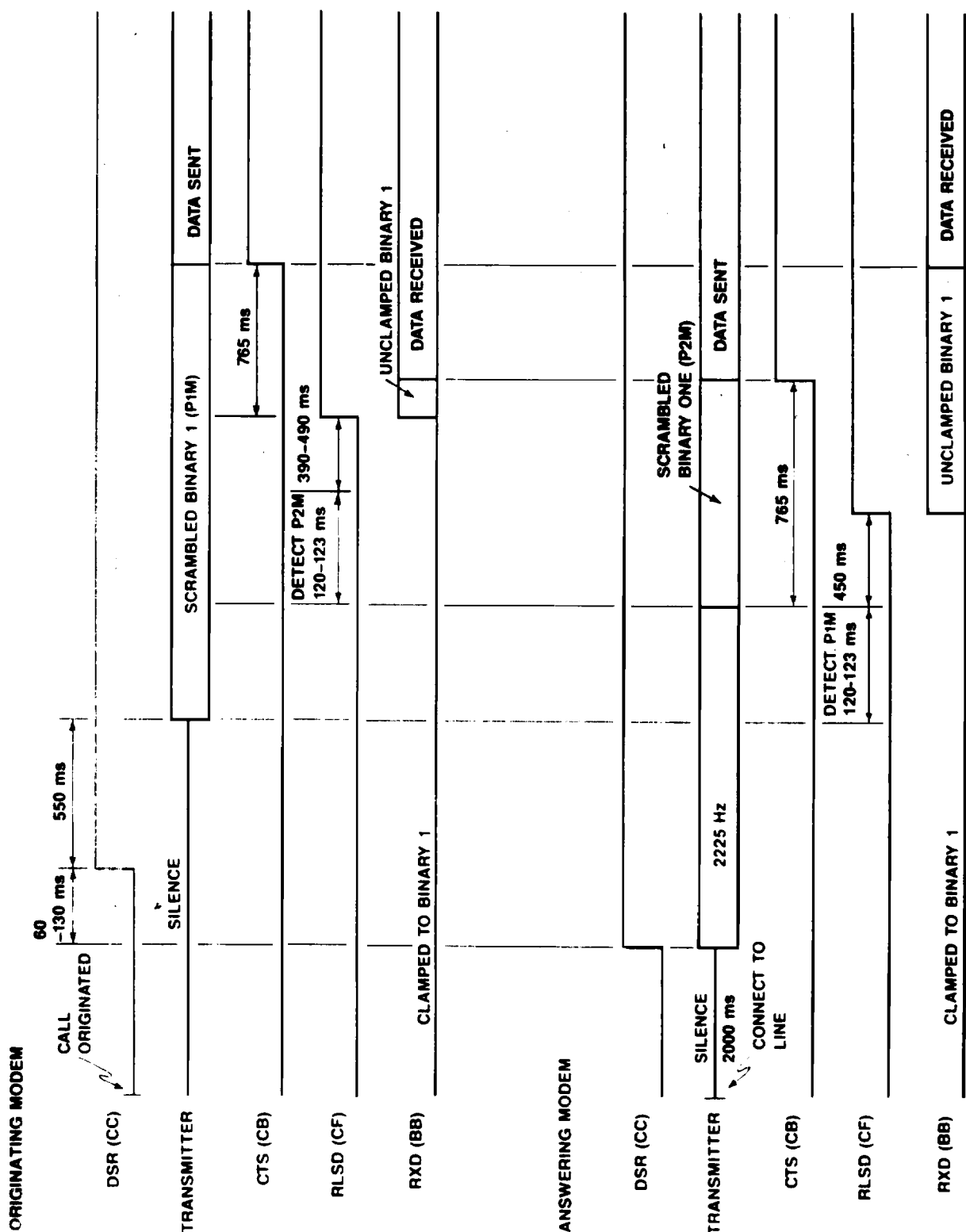Figure 6-8. Bell 212A 1200 bps Connect Sequence - Std.

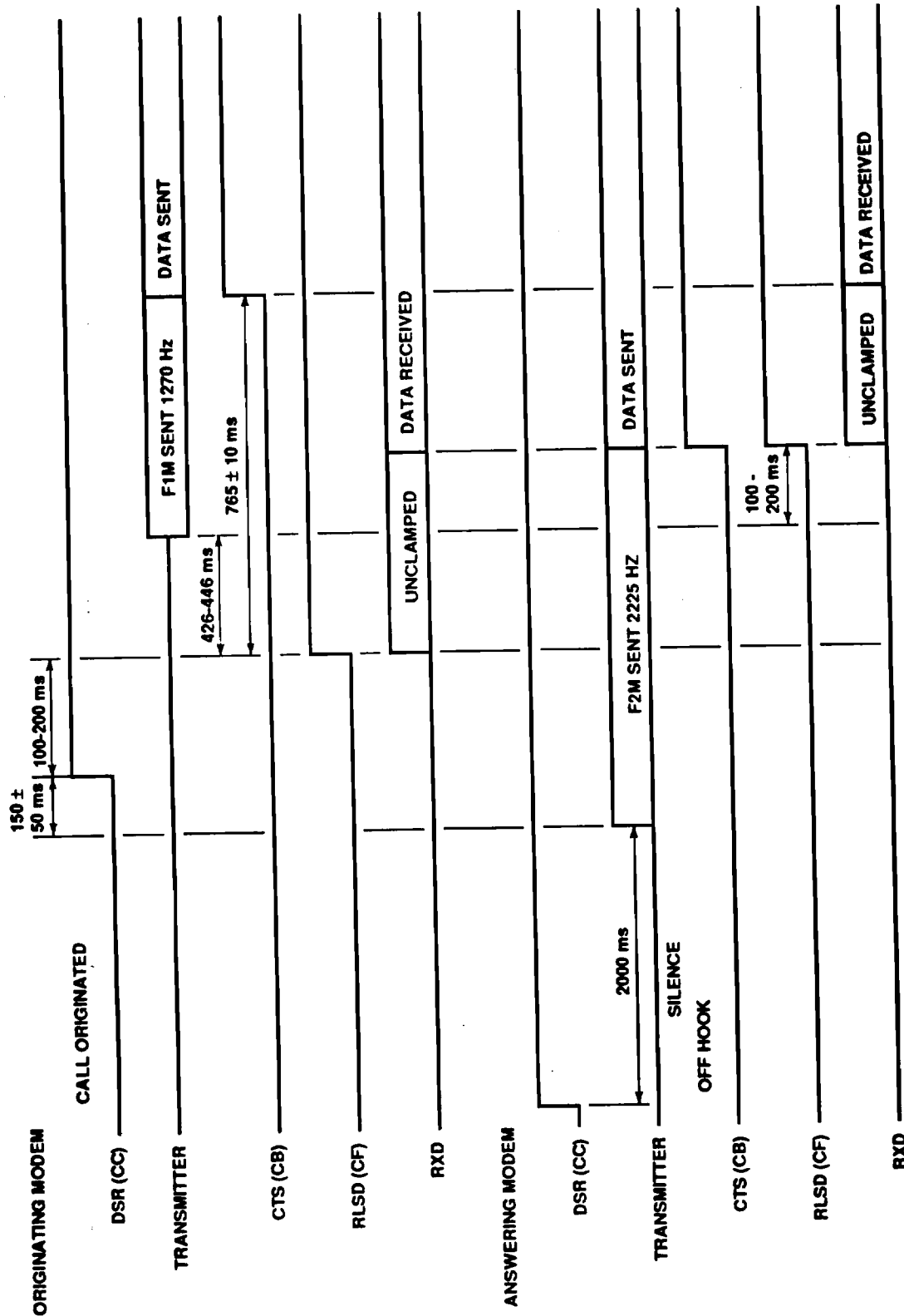Figure 6-9. Bell 212A 1200 bps Connect Sequence - Impl.

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Figure 6-10. Bell 103 300 bps Connect Sequence - Std.
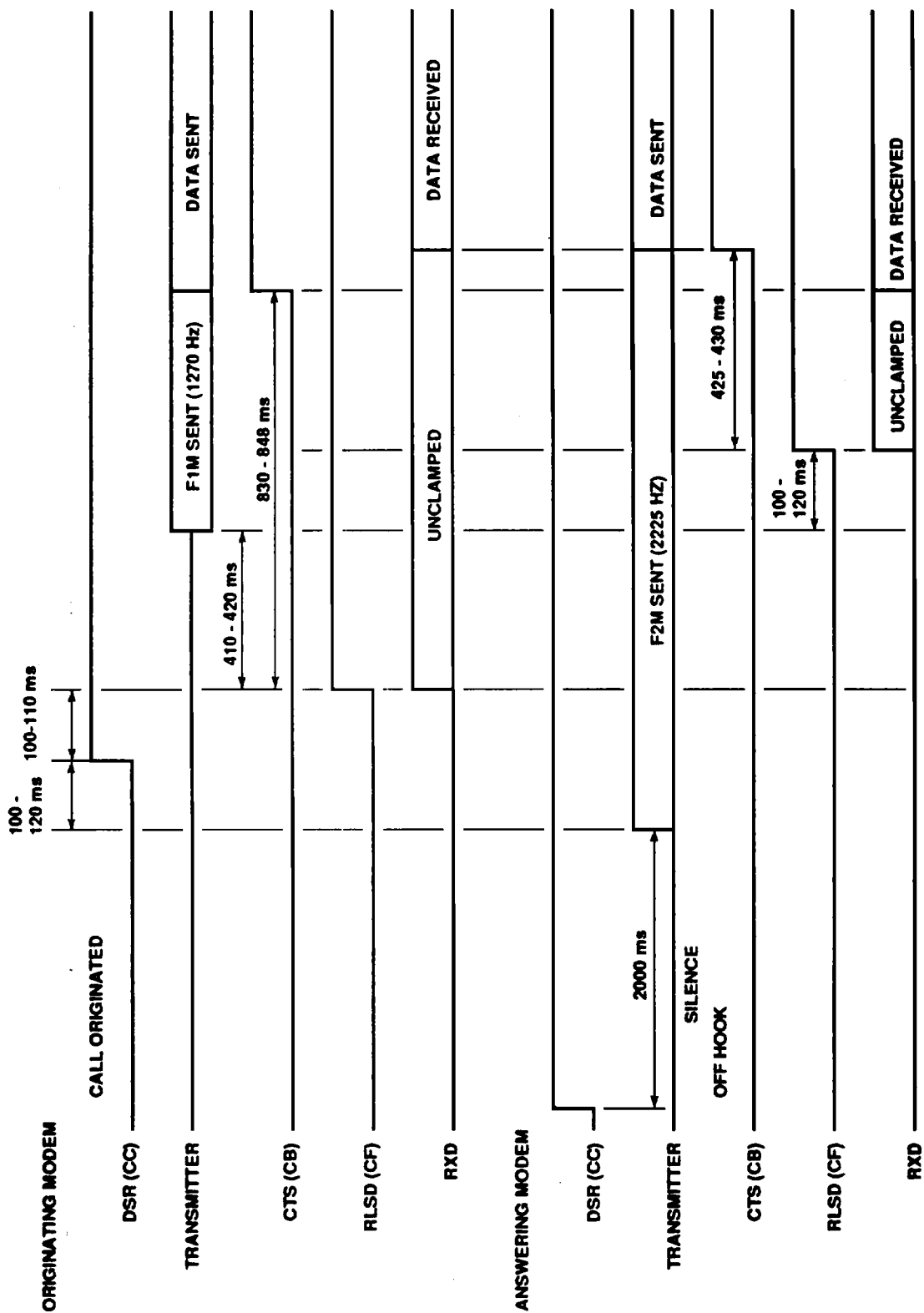
Figure 6-11. Bell 103 300 bps Connect Sequence - Impl.
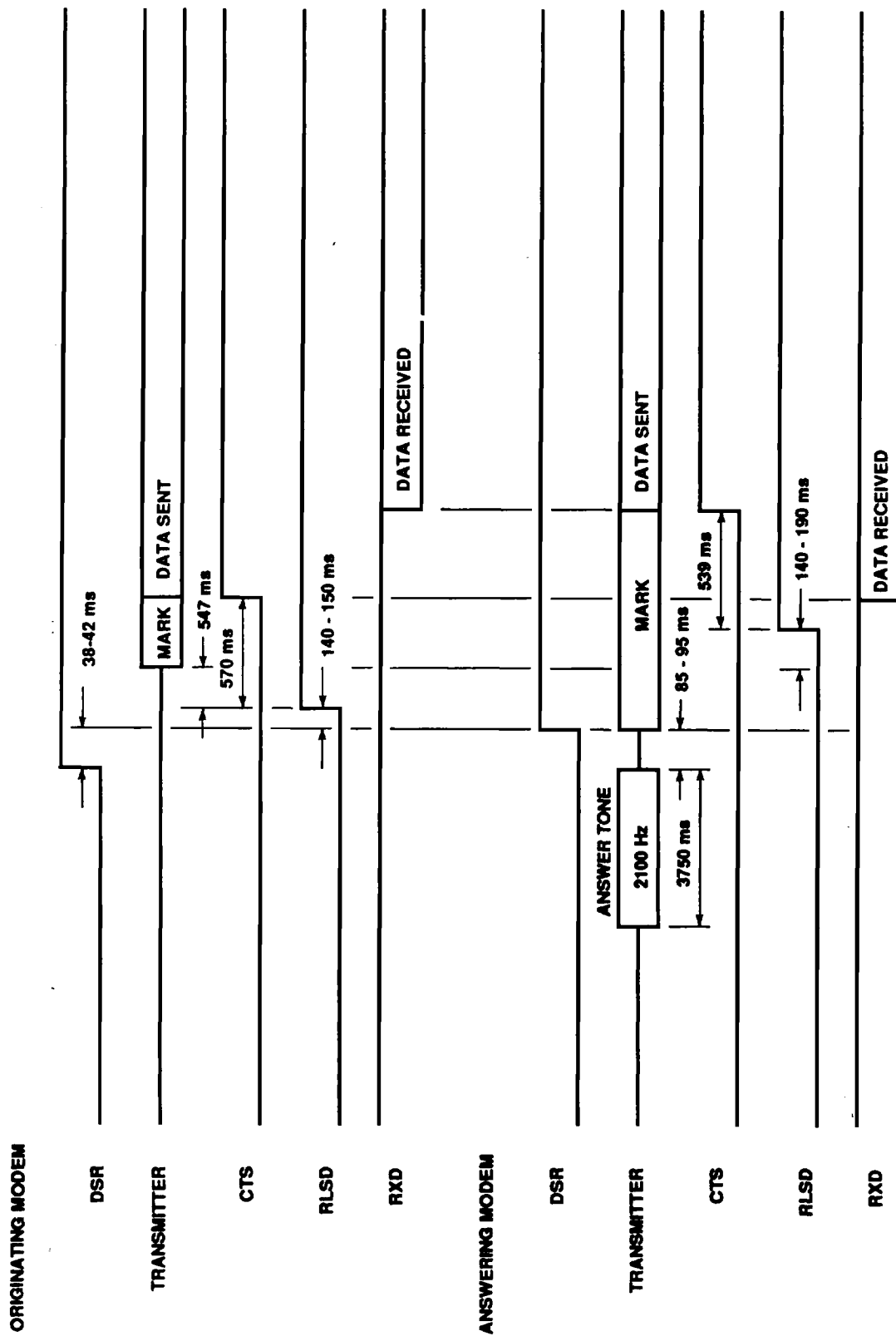
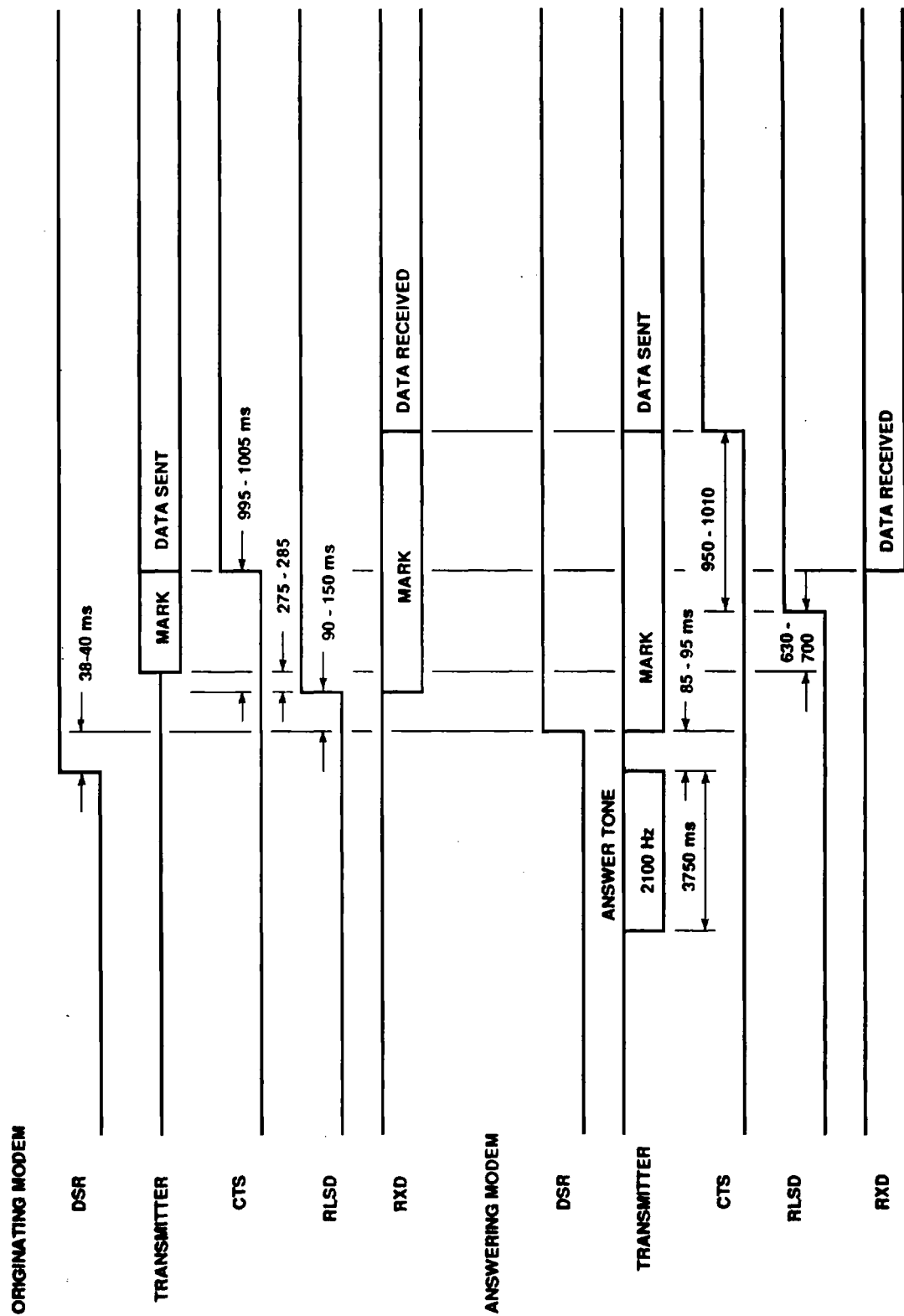Figure 6-12. V.25/V.21 Call Establishment Timing
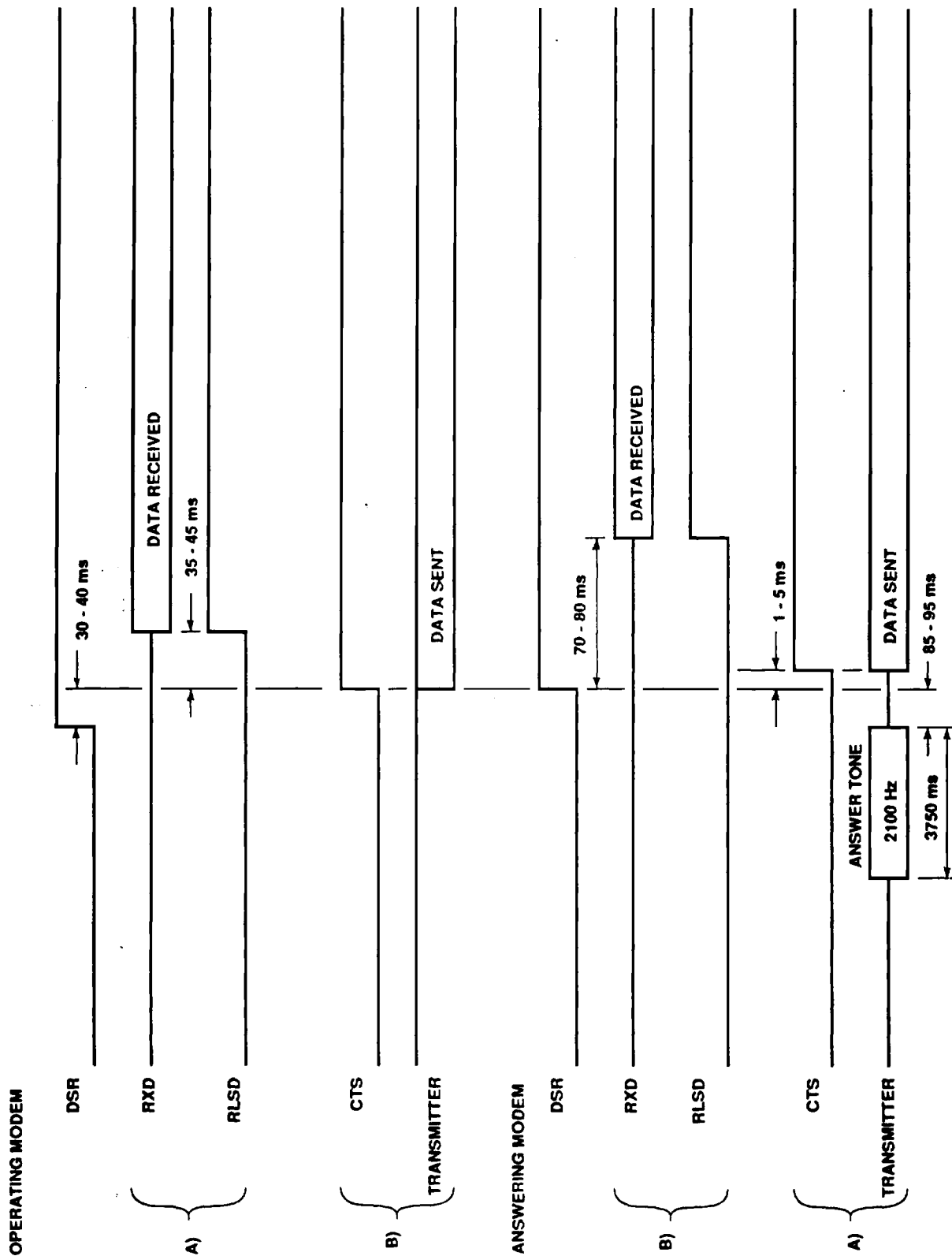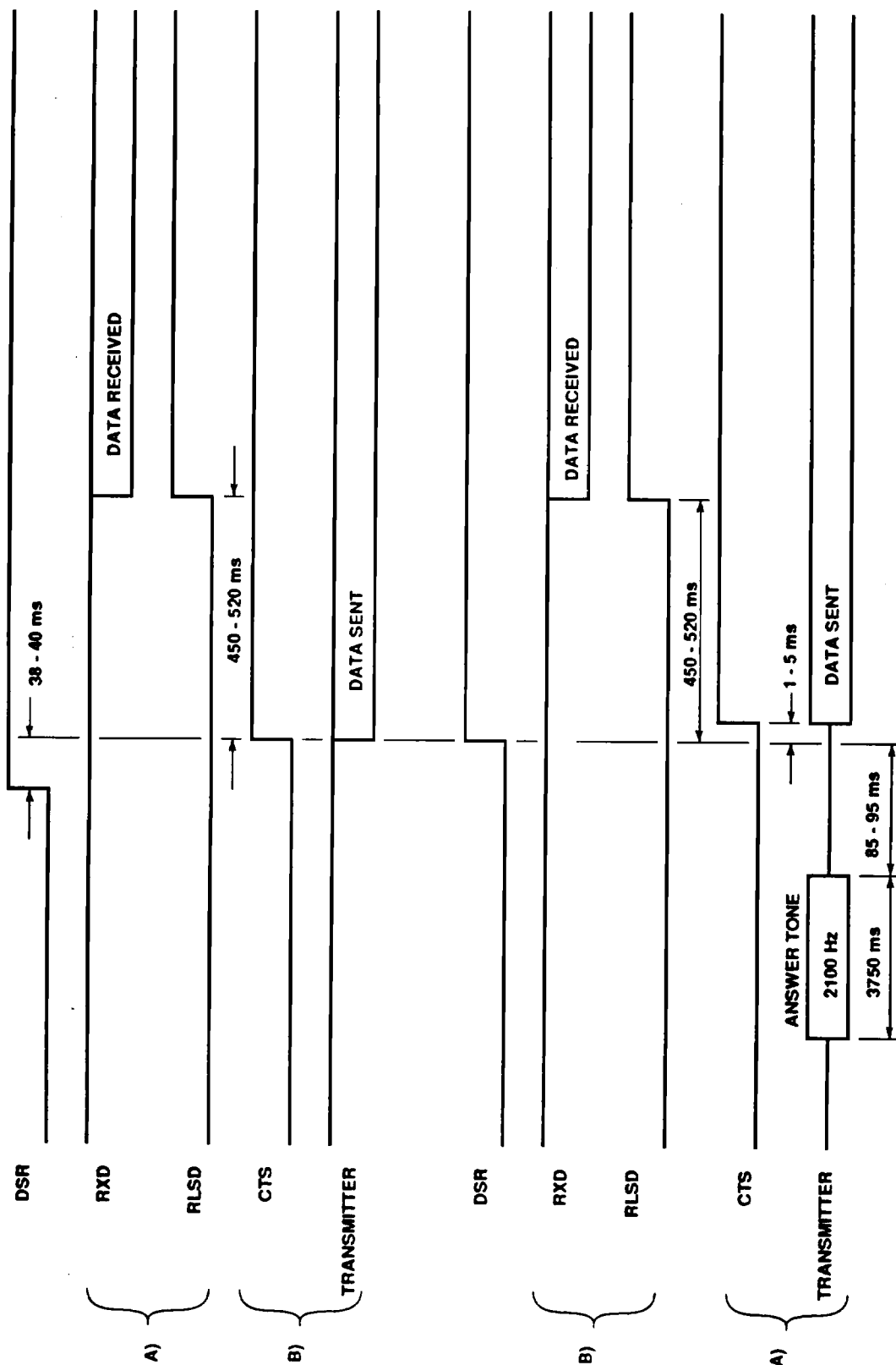
Figure 6-13. V.25/V.23 Call Estab. - 1200 bps, 75 bps

Figure 6-14. V.25/V.23 Call Estab. - 1200 bps Half-Duplex

Figure 6-15. V.25/V.23 Call Estab. - 75 bps Half-Duplex

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7. AUTOMATIC MODE DETECTION RECONFIGURATION

The modem supports CCITT recommendations V.22 bis, V.22, V.21, and V.23, as well as Bell 212 (1200 bps) and Bell 103. V.22 bis, V.22, Bell 212, and Bell 103 define handshake sequences for modems using those configurations. In instances where the host does not know what type of modem is located at the remote end, a method of automatic detection and reconfiguration is needed.

Several methods of automatic mode detection and reconfiguration are possible.

One method makes use of the zero-crossing counter (available at XRAM address 3B, XCR = 1) to determine the frequency of the incoming signal.

A second method, presented in the section, makes use of the digital filters available in each mode. More information on the digital filters and the default frequency detection values can be found under "Diagnostic Data Scaling" in section 3. An automatic mode detection/reconfiguration scheme is shown for both originate and answer modes in Figures 7-1 and 7-2, respectively. This scheme can be used to detect and configure all supported CCITT and Bell modes.

Note: In V.22 bis (2400 bps), some modems require scrambled Mark in addition to the amount allowed by the CCITT V.22 bis handshake. Additional scrambled Marks can be provided by the host by not raising CTS to the DTE until an amount of time after connection is established.
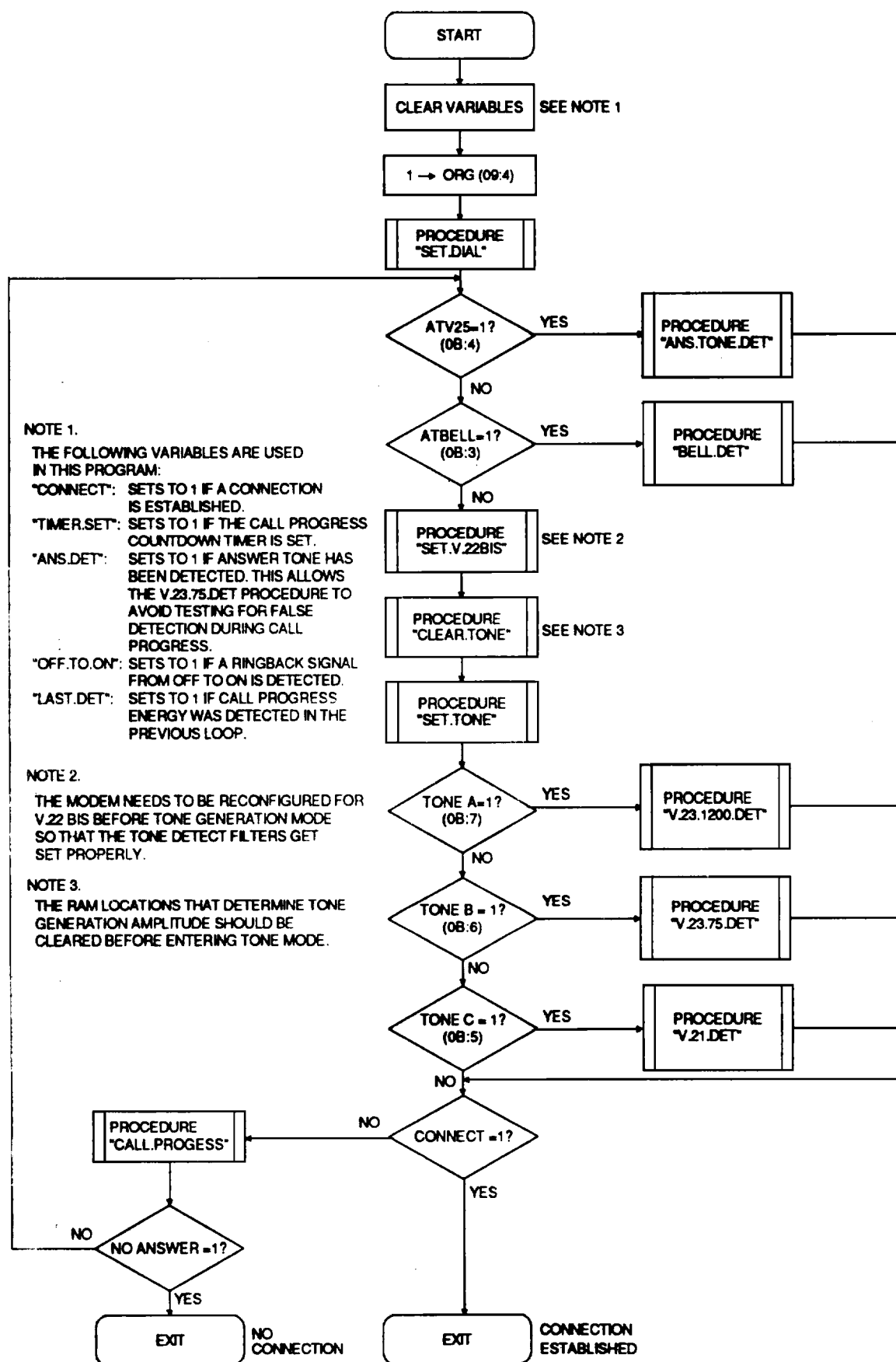
```
                              ┌──────────────┐
                              │    START     │
                              └──────┬───────┘
                                     │
                          ┌──────────────────┐
                          │ CLEAR VARIABLES  │  SEE NOTE 1
                          └──────────┬───────┘
                                     │
                          ┌──────────────────┐
                          │  1 → ORG (09:4)  │
                          └──────────┬───────┘
                                     │
                          ┌──────────────────┐
                          │    PROCEDURE     │
                          │   "SET.DIAL"     │
                          └──────────┬───────┘
```
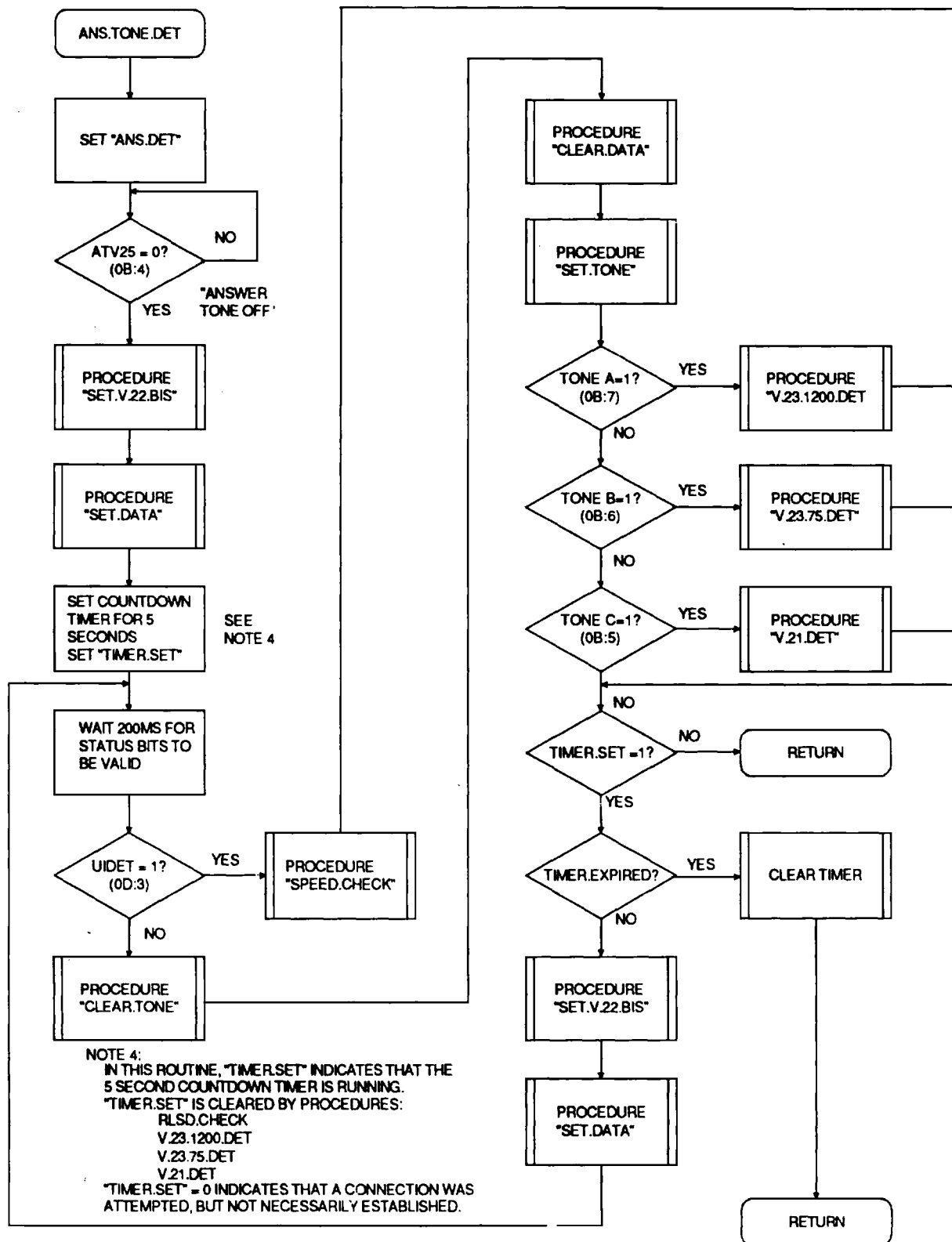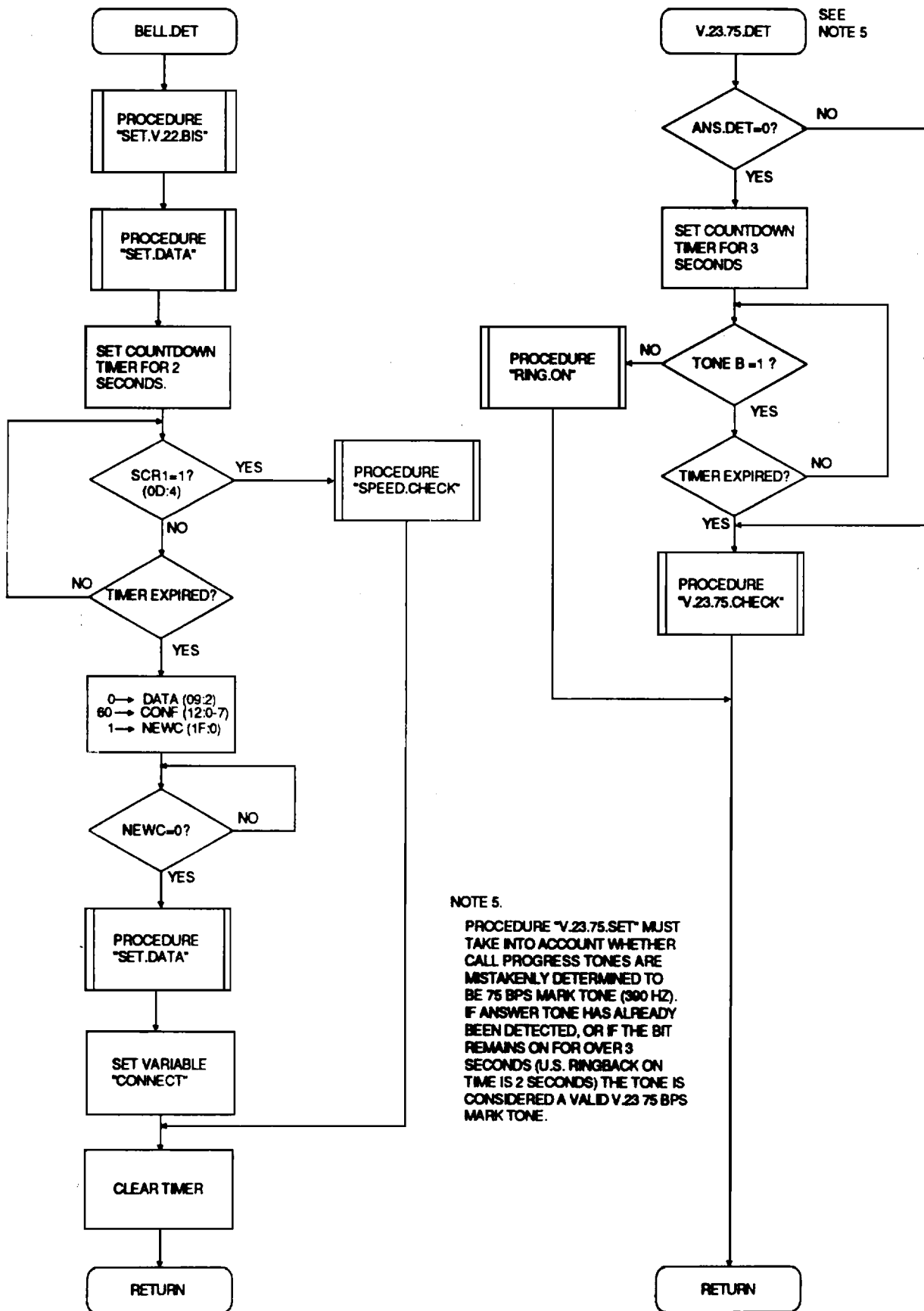
NOTE 1.

THE FOLLOWING VARIABLES ARE USED IN THIS PROGRAM:

"CONNECT": SETS TO 1 IF A CONNECTION IS ESTABLISHED.

"TIMER.SET": SETS TO 1 IF THE CALL PROGRESS COUNTDOWN TIMER IS SET.

"ANS.DET": SETS TO 1 IF ANSWER TONE HAS BEEN DETECTED. THIS ALLOWS THE V.23.75.DET PROCEDURE TO AVOID TESTING FOR FALSE DETECTION DURING CALL PROGRESS.

"OFF.TO.ON": SETS TO 1 IF A RINGBACK SIGNAL FROM OFF TO ON IS DETECTED.

"LAST.DET": SETS TO 1 IF CALL PROGRESS ENERGY WAS DETECTED IN THE PREVIOUS LOOP.

NOTE 2.

THE MODEM NEEDS TO BE RECONFIGURED FOR V.22 BIS BEFORE TONE GENERATION MODE SO THAT THE TONE DETECT FILTERS GET SET PROPERLY.

NOTE 3.

THE RAM LOCATIONS THAT DETERMINE TONE GENERATION AMPLITUDE SHOULD BE CLEARED BEFORE ENTERING TONE MODE.

Decision/procedure flow:

- ATV25=1? (0B:4) — YES → PROCEDURE "ANS.TONE.DET"; NO →
- ATBELL=1? (0B:3) — YES → PROCEDURE "BELL.DET"; NO →
- PROCEDURE "SET.V.22BIS" (SEE NOTE 2)
- PROCEDURE "CLEAR.TONE" (SEE NOTE 3)
- PROCEDURE "SET.TONE"
- TONE A=1? (0B:7) — YES → PROCEDURE "V.23.1200.DET"; NO →
- TONE B = 1? (0B:6) — YES → PROCEDURE "V.23.75.DET"; NO →
- TONE C = 1? (0B:5) — YES → PROCEDURE "V.21.DET"; NO →
- CONNECT =1? — NO → PROCEDURE "CALL.PROGESS"; YES → EXIT (CONNECTION ESTABLISHED)
- NO ANSWER =1? — NO → (loop back); YES → EXIT (NO CONNECTION)

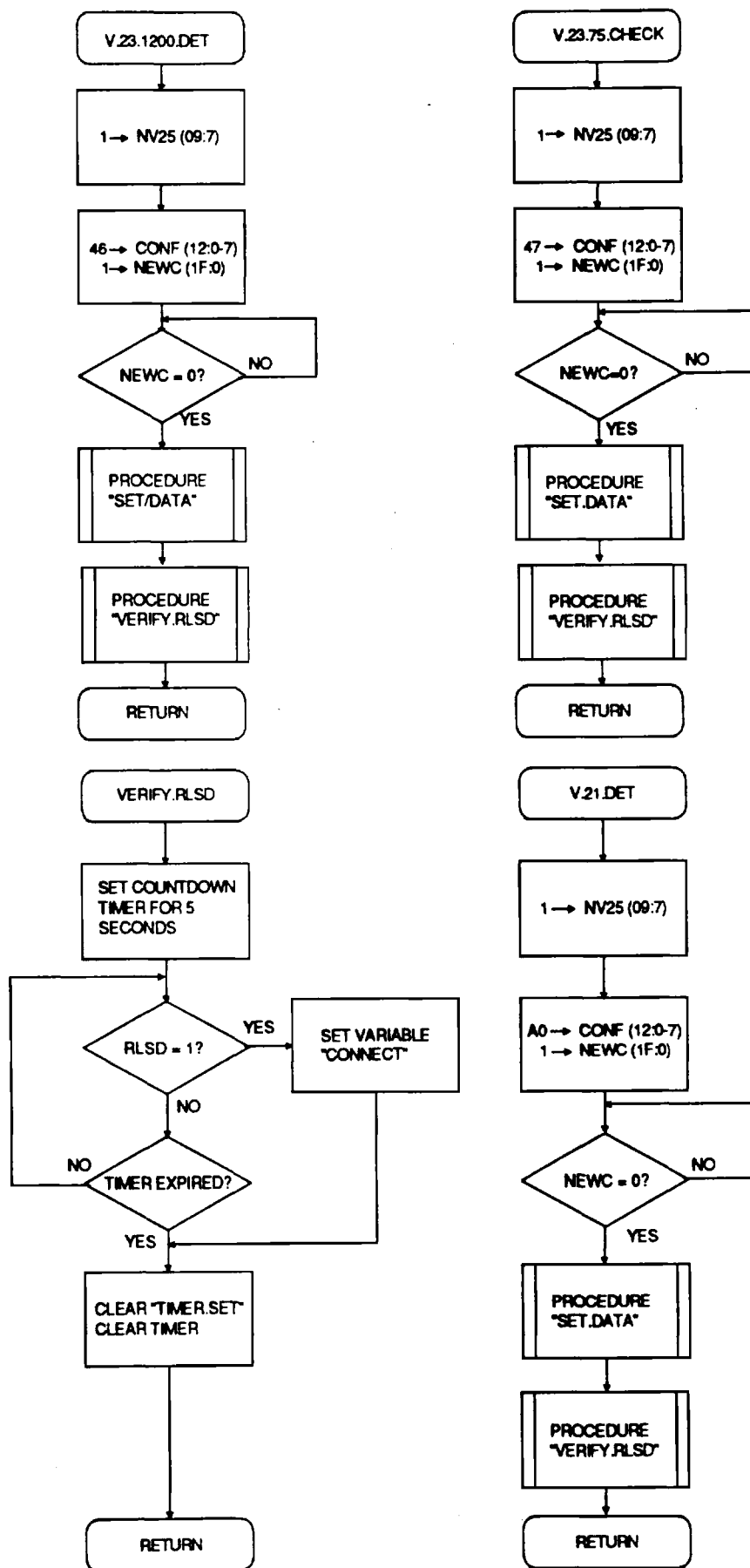**Figure 7-1. Auto Detection/Reconfiguration-Originate**
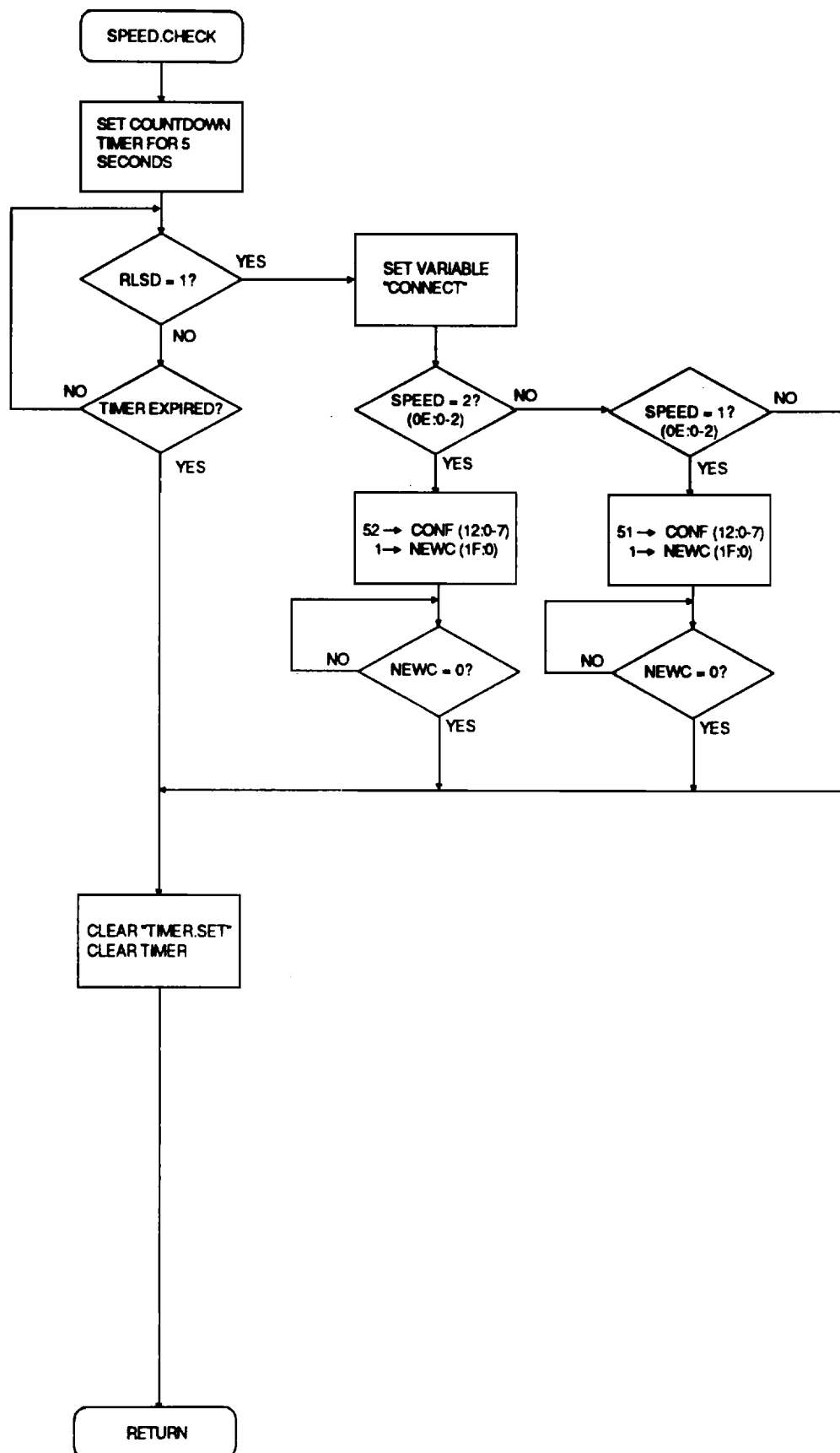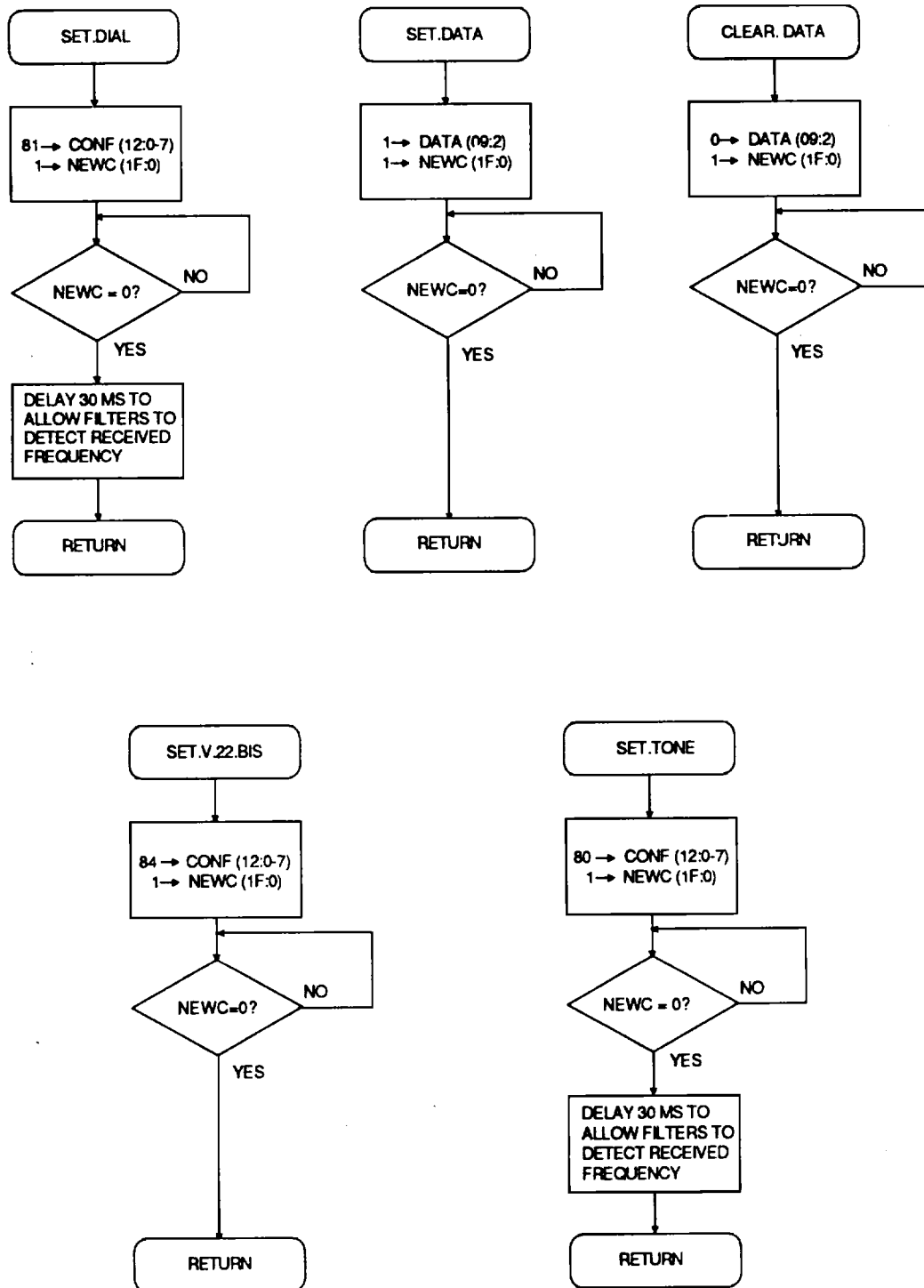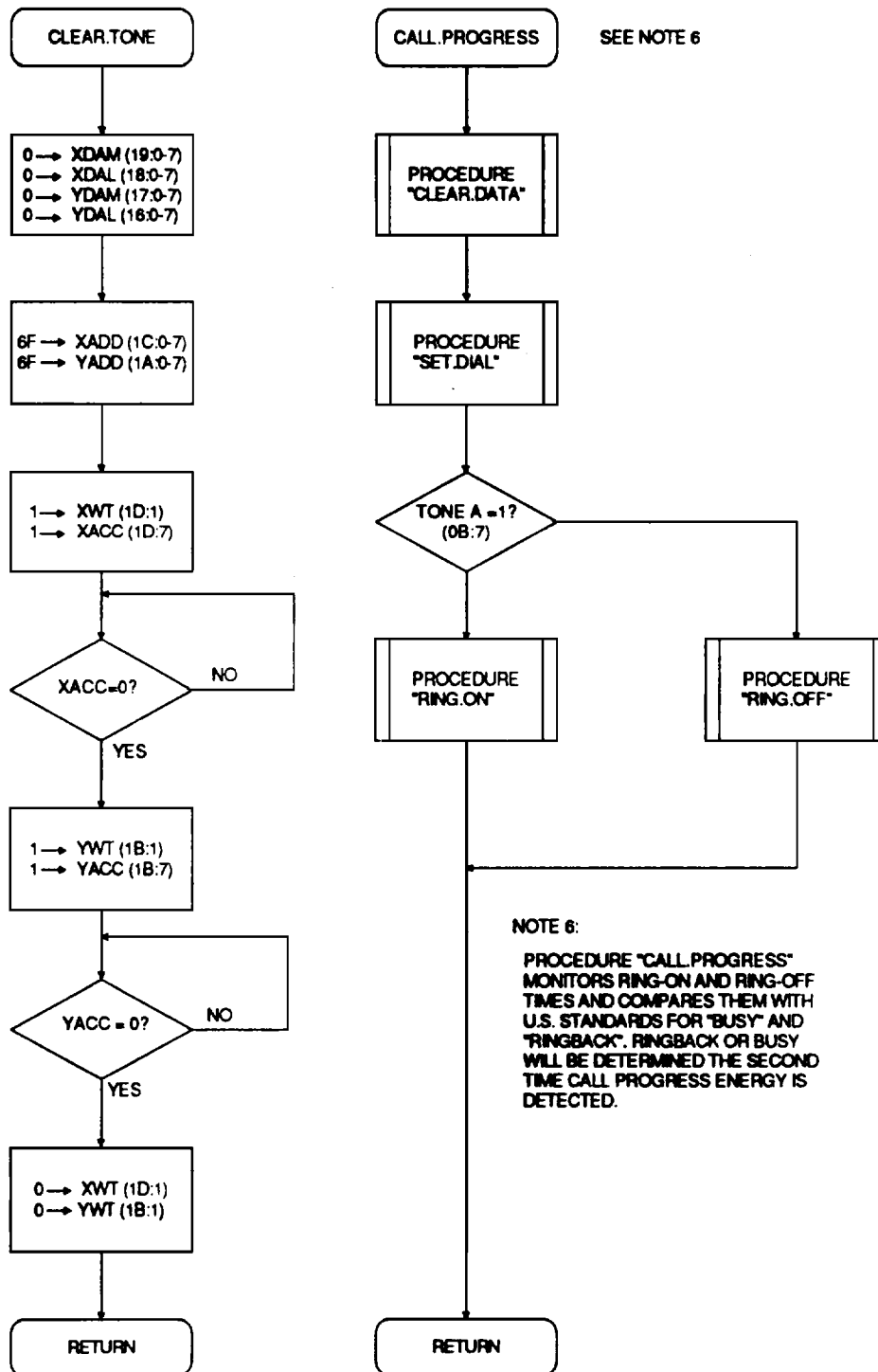
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Figure 7-1. Auto Detection/Reconfiguration-Originate (Cont)

Figure 7-1. Auto Detection/Reconfiguration-Originate (Cont)

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Figure 7-1. Auto Detection/Reconfiguration-Originate (Cont)

Figure 7-1. Auto Detection/Reconfiguration-Originate (Cont)

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SET.DIAL

81 → CONF (12:0-7)
1 → NEWC (1F:0)

NEWC = 0?   NO

YES

DELAY 30 MS TO
ALLOW FILTERS TO
DETECT RECEIVED
FREQUENCY

RETURN

SET.DATA

1 → DATA (09:2)
1 → NEWC (1F:0)

NEWC=0?   NO

YES

RETURN

CLEAR. DATA

0 → DATA (09:2)
1 → NEWC (1F:0)

NEWC=0?   NO

YES

RETURN

SET.V.22.BIS

84 → CONF (12:0-7)
1 → NEWC (1F:0)

NEWC=0?   NO

YES

RETURN

SET.TONE

80 → CONF (12:0-7)
1 → NEWC (1F:0)

NEWC = 0?   NO

YES

DELAY 30 MS TO
ALLOW FILTERS TO
DETECT RECEIVED
FREQUENCY

RETURN

Figure 7-1. Auto Detection/Reconfiguration-Originate (Cont)

CLEAR.TONE

0 → XDAM (19:0-7)
0 → XDAL (18:0-7)
0 → YDAM (17:0-7)
0 → YDAL (16:0-7)

6F → XADD (1C:0-7)
6F → YADD (1A:0-7)

1 → XWT (1D:1)
1 → XACC (1D:7)

XACC=0? — NO

YES

1 → YWT (1B:1)
1 → YACC (1B:7)

YACC = 0? — NO

YES

0 → XWT (1D:1)
0 → YWT (1B:1)

RETURN

CALL.PROGRESS   SEE NOTE 6

PROCEDURE "CLEAR.DATA"

PROCEDURE "SET.DIAL"

TONE A =1? (0B:7)

PROCEDURE "RING.ON"

PROCEDURE "RING.OFF"

NOTE 6:

PROCEDURE "CALL.PROGRESS" MONITORS RING-ON AND RING-OFF TIMES AND COMPARES THEM WITH U.S. STANDARDS FOR "BUSY" AND "RINGBACK". RINGBACK OR BUSY WILL BE DETERMINED THE SECOND TIME CALL PROGRESS ENERGY IS DETECTED.

RETURN

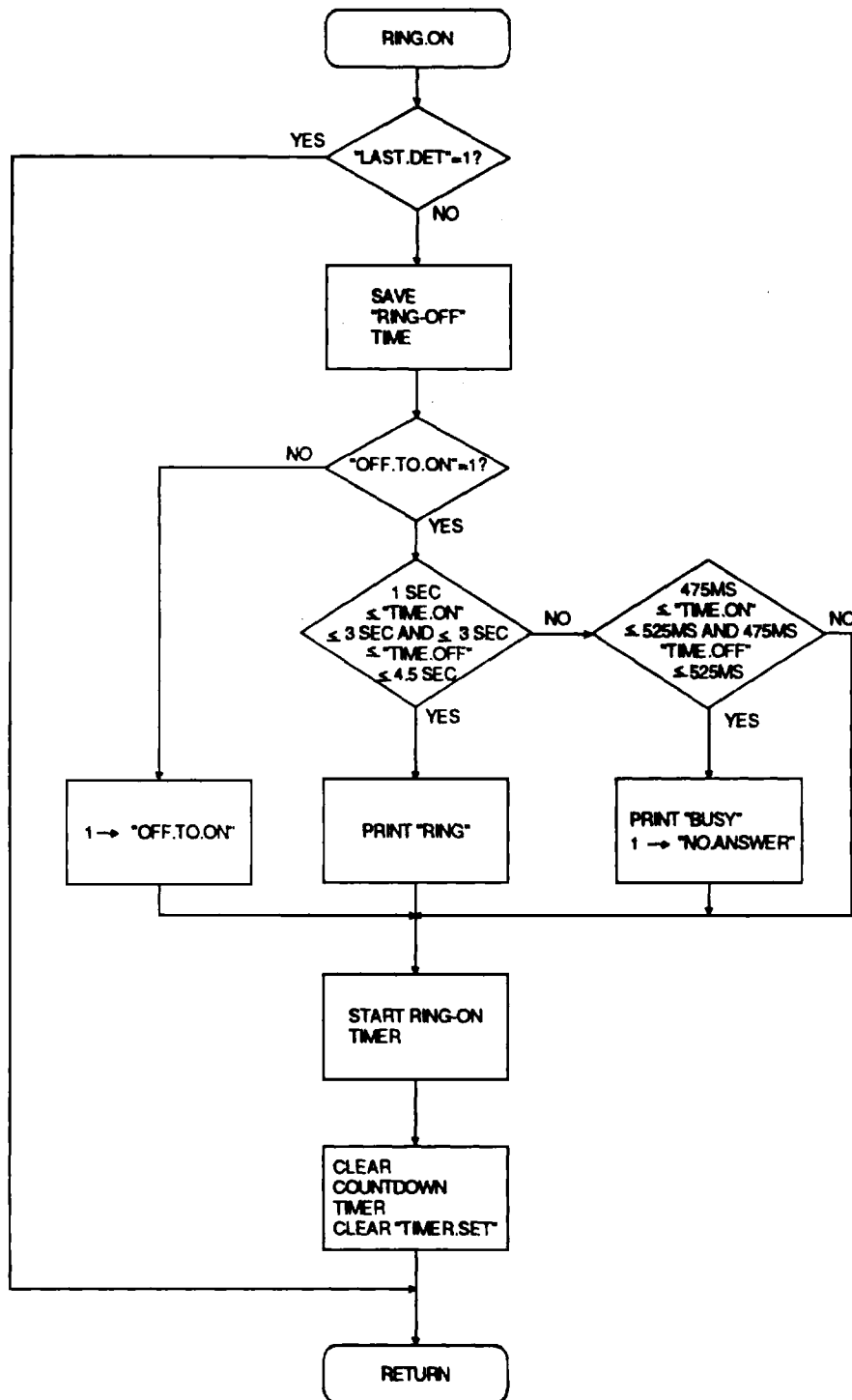**Figure 7-1. Auto Detection/Reconfiguration-Originate (Cont)**

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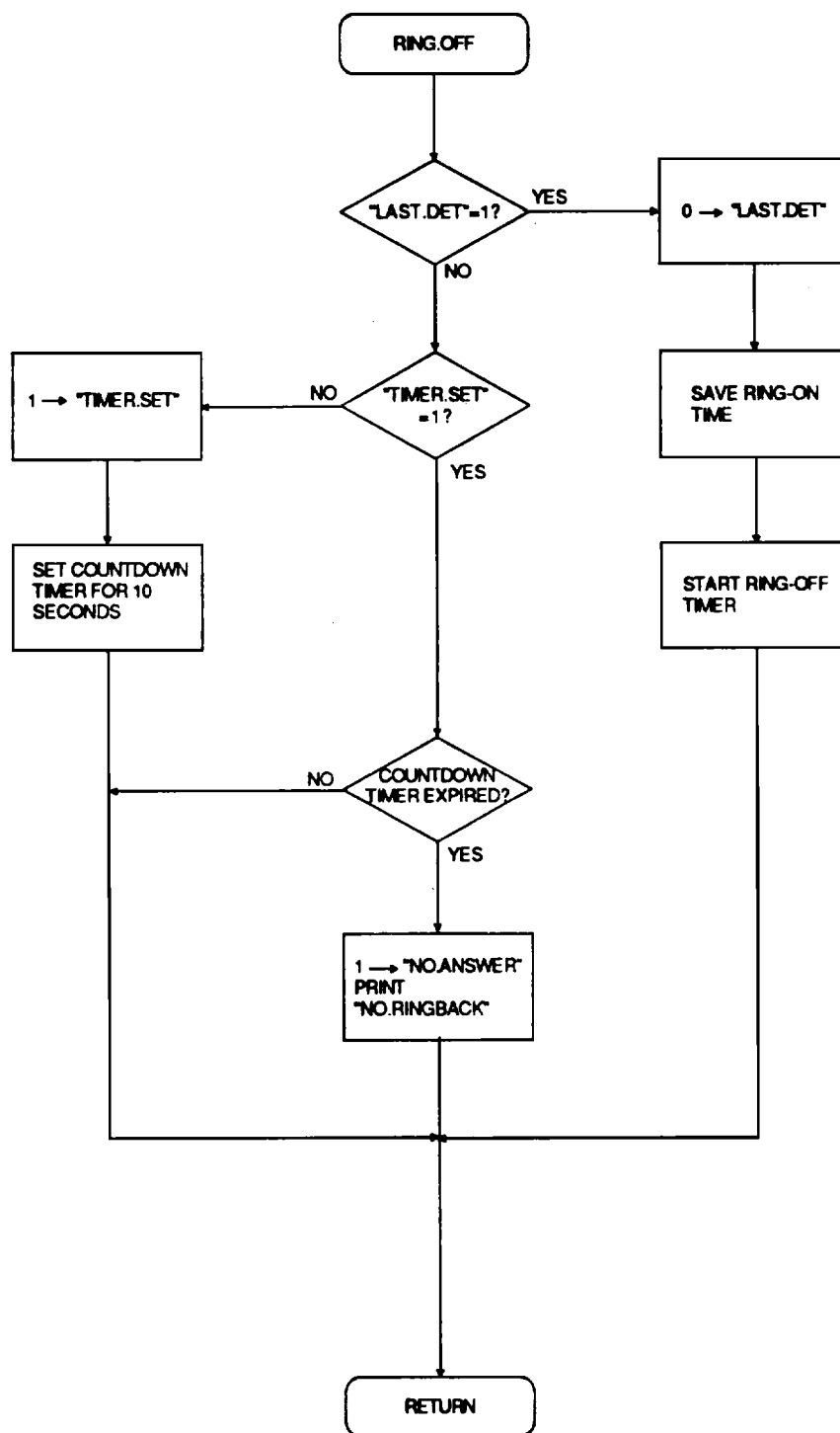Figure 7-1. Auto Detection/Reconfiguration-Originate (Cont)

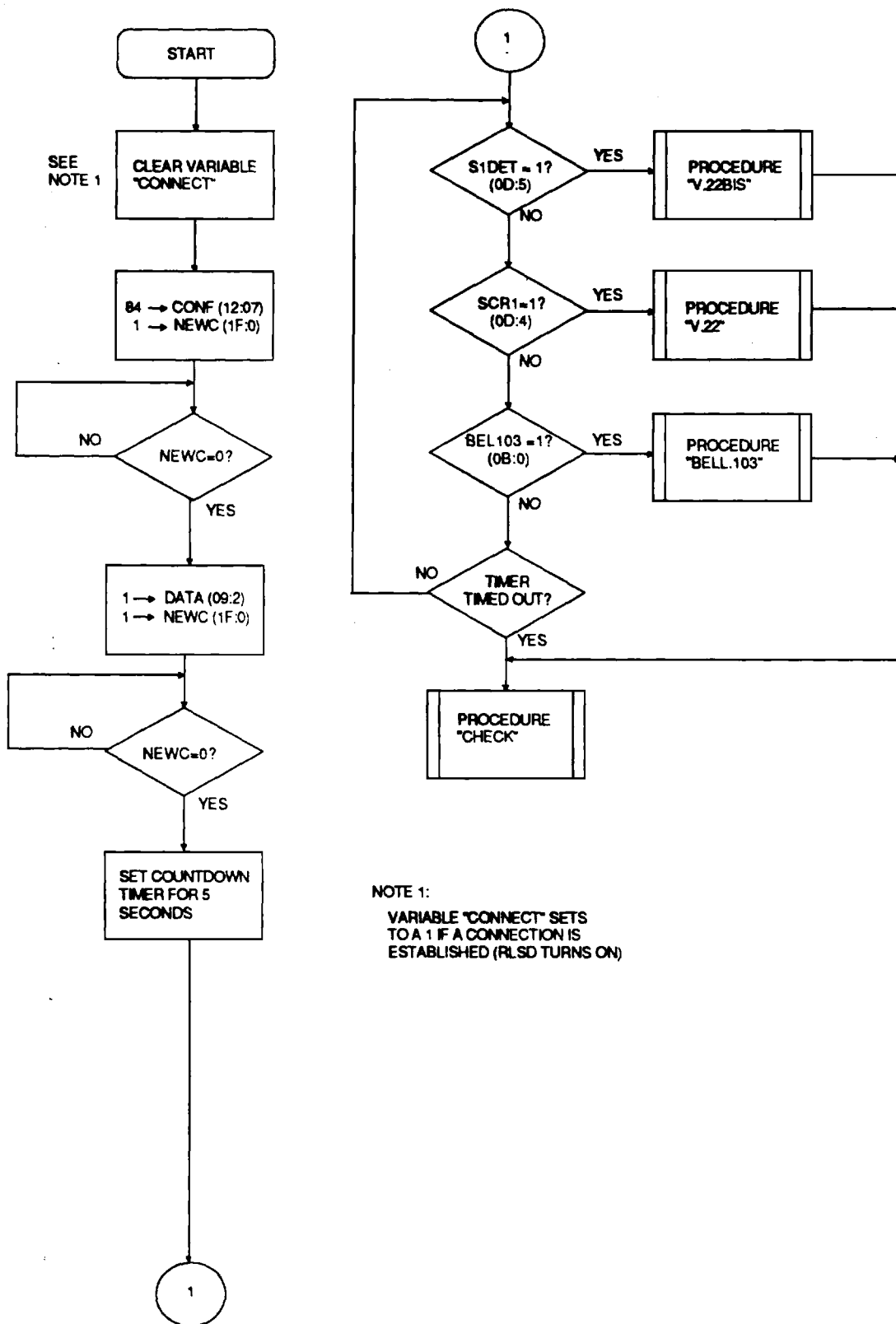**Figure 7-1. Auto Detection/Reconfiguration-Originate (Cont)**
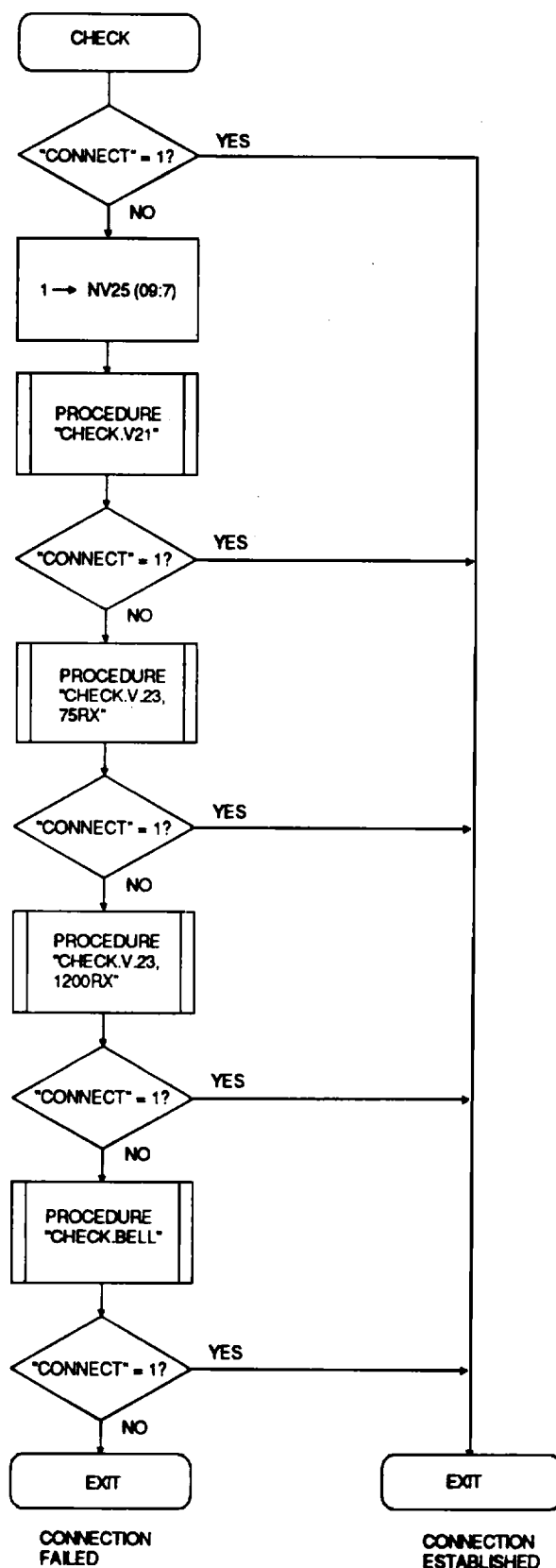
Figure 7-2. Auto Detection/Reconfiguration-Answer

Figure 7-2. Auto Detection/Reconfiguration-Answer (Cont)

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